CMOS Phased Array Transceiver Technology for 60 GHz Wireless Applications

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***Abstract*—Based on the indoor radio-wave propagation analysis, and the fundamental limits of CMOS technology it is shown that phased array technology is the ultimate solution for the radio and physical layer of the millimeter wave multi-Gb/s wireless networks. A low-cost, single-receiver array architecture with RF phase-shifting is proposed and design, analysis and measurements of its key components are presented. A high-gain, two-stage, low noise amplifier in 90 nm-CMOS technology with more than 20 dB gain over the 60 GHz spectrum is designed. Furthermore, a broadband analog phase shifter with a linear phase and low insertion loss variation is designed, and its measured characteristics are presented. Moreover, two novel beamforming techniques for millimeter wave phased array receivers are developed in this paper. The performance of these methods for line-of-sight and multipath signal propagation conditions is studied. It is shown that one of the proposed beamforming methods has an excess gain of up to 14 dB when the line of sight link is obstructed by a human.**

***Index Terms*—Beam-forming, CMOS, millimeter wave, phased array antenna, 60 GHz.**

I. Introduction

In the endless pursuit of higher bandwidth for wireless communications, researchers and industries are becoming more and more interested in millimeter wave (MMW) spectrum [1]–[7]. Recently, 60 GHz frequency band has been released and proposed for short-range wireless applications such as wireless personal area network (WPAN) [8], [9], and wireless multimedia/high-definition (HD) streaming. IEEE 802.15.3 task group 3c (TG3c) is working on standardization of this frequency band for short range wireless applications. At the same time, Wireless HD Consortium is defining a wireless protocol to create a 60 GHz wireless video network for consumer electronic audio and video devices [10]. High-volume markets for 60 GHz systems are promising if compact, low cost, high performance transceivers become available.

Manuscript received July 16, 2008; revised August 16, 2009; accepted November 10, 2009. Date of publication January 22, 2010; date of current version April 07, 2010. This work was supported in part by the National Science and Engineering Research Council (NSERC) of Canada, RIM (Research In Motion), Ontario Center of Excellence (OCE), and in part by Nortel.

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Digital Object Identifier 10.1109/TAP.2010.2041140

Complementary metal-oxide semiconductor (CMOS) is the dominating technology for most wireless products below 10 GHz. This dominance has been achieved by reliability, low cost, and high device count advantages of CMOS compared to the other semiconductor technologies such as SiGe and GaAs. Today, with the aggressive scaling of gate length, CMOS technology is pushing further into the MMW region. Moreover, CMOS is the most promising technology for system-on-chip design, because it enables integration of the analog RF circuits as well as the digital signal processing and baseband circuits in the lowest possible chip area, which leads to a lower cost and more compact solution. Therefore, the nano-scale CMOS technology, such as 90 nm, 65 nm and 45 nm, offers commercial MMW solutions for short range and high data rate applications. However, several system and circuit level challenges must be met, such as lack of the efficient and low cost antenna and packaging solutions, low output power and nonlinearity of power amplifiers, severe path loss, shadowing loss, limited gain of the low noise amplifier (LNA) and its high noise figure. For a wide range of emerging applications in the 60 GHz spectrum, as will be discussed in this paper, use of multiple antennas with beam steering capabilities is a key enabling technology to address most of these challenges. However the efficiency of a phased array depends on the performance of power amplifier or LNA as well as phase shifter. Furthermore, to lower the overall cost, all microwave components must be implemented in a low-cost technology and possibly on a single chip. Therefore one objective of this paper is to present a high-performance phase shifter and LNA in CMOS technology.

So far, the reported MMW systems at 52, 60 and 77 GHz bands in CMOS and SiGe are either simple receiver [4], [5], [11], two-element receiver [12], transmitter only [13], [14], or transceivers which are not able to meet some of the above mentioned challenges [2], [15]. Moreover, the proposed phased array solutions are costly and complex requiring large chip area and high power consumption [6], [12]. The situation is worsened if a large number of array elements are needed to meet the link budget and network coverage specification.

In this paper, feasibility, system architecture and the key components of a low-cost and low-noise CMOS phased array transceiver for a broadband wireless network at 60 GHz, are analyzed. Another objective of this paper is to show that the key microwave components, i.e. high-gain LNA and linear phase shifter, can be implemented in CMOS technology at 60 GHz. Furthermore, we will show that a 9 or 16 element CMOS phased array can achieve the required signal to noise ratio for multi-Gb/s wireless communication in a picocell (such as a regular office), if a powerful beamforming algorithm is used.

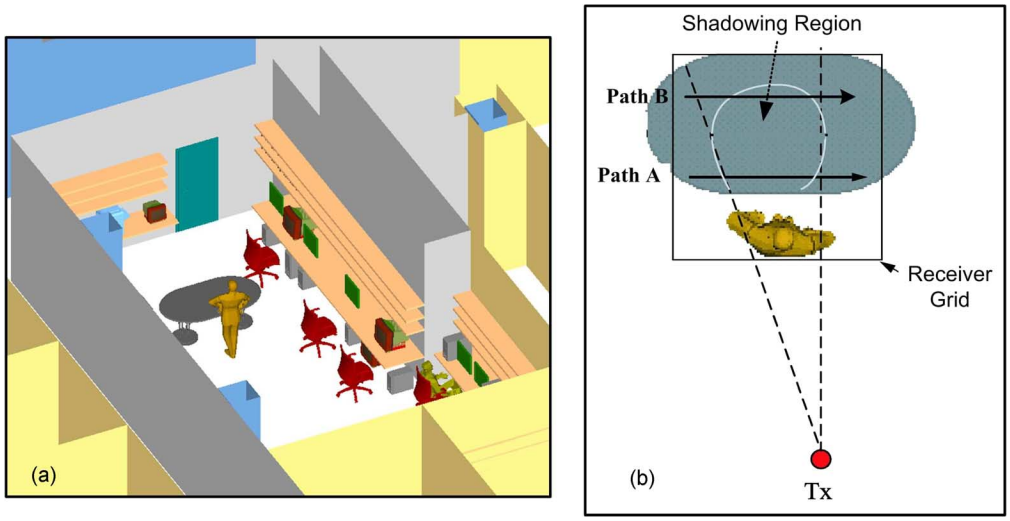

Fig. 1. (a) Simulated 3D view, and (b) top view of the propagation environment (CAD Lab at the University of Waterloo).

The organization of this paper is as follows. In Section II the indoor 60 GHz propagation channel is studied and a test set-up for measuring the shadowing loss of a human body is described. A low-cost architecture for 60 GHz phased array transceiver is presented in Section III and the design, analysis and measurements of its key components are presented in Section IV. Finally, novel beamforming algorithms for the phased array receiver are introduced in Section V and Section VI concludes this paper.

II. Indoor 60 GHz Propagation Channel: Modeling and Measurement

A. Modeling

Indoor propagation at MMW frequencies can be modeled using geometrical optics (GO) ray-tracing method enhanced by uniform asymptotic diffraction theories and experimental models. The reliability of channel characterization results obtained by ray-tracing method at microwave frequencies has been confirmed by different measurements [16]–[18]. For indoor applications at 60 GHz, the high penetration loss of the material isolates adjacent rooms and significantly limits the received interference, so only those objects inside the room need to be included in ray-tracing simulation. In this in-room propagation channel, both line of sight (LOS) and non line of sight (NLOS) rays must be considered. The NLOS rays are caused by reflections from the objects inside the room as well as some significant first order diffracted rays. Furthermore, propagation loss in the ray-tracing modeling consists of free-space loss according to Friis formula, gaseous loss, and reflection, transmission and diffraction losses.

In this work, a 3D ray-tracing modeling (GO plus diffraction) is employed to assess the signal coverage at 60 GHz for a regular office area. The CAD Laboratory, located in the EIT building at the University of Waterloo, is used as a typical indoor wireless environment (see Fig. 1(a)). The lab is furnished with tables, chairs and shelves mostly constructed of wooden and plastic material. The walls consist of layers of different material such as plasterboard, concrete, and wood. Moreover, various electronic equipments such as computers, printers and test devices are placed in this lab. The empirical data reported in [19] and [20] is used to calculate the reflection coefficients of the material. Moreover, to evaluate the human body shadowing effect the measured permittivity data for biological tissues in [21] is used. Table I summarizes the measured permittivity data at 60 GHz used in this work.

TABLE I
Measured Permittivity of Indoor Materials at 60 GHz

Type	Complex ϵ_r
Acrylic Glass	$2.5298 - j2.5298$
Chipboard	$2.8556 - j0.1586$
Concrete	$6.1326 - j0.3014$
Glass	$5.2839 - j0.2538$
Plasterboard	$2.8096 - j0.0461$
Wood	$1.5671 - j0.0962$
Human Body	$13.2 - j10.4$

The transmitter antenna in Fig. 1 is located 10 cm below the center of the ceiling (facing down) which is 3.45 m above the floor. The receiver is located on a wooden table 75 cm above the floor. To simulate the shadowing effect, a human-body blocks the LOS path between the transmitter and the receiver as shown in Fig. 1(b). To model a mobile user (portable end-device), the receiver antenna moves within a 2 m $\times$ 1.75 m grid located 1 m above the floor (25 cm above the table). The resolution of the grid-cells varies from $\lambda/5$ to $\lambda/2$.

Fig. 2 demonstrates the ray-tracing results at 60 GHz for the rectangular grid in front of the human body in Fig. 1. The human body model is 1.8 m tall centered at (-0.5 m, 1.4 m, 2.54 m) relative to the transmitter antenna. The white area in Fig. 2(a) illustrates the relative opaqueness of the human body at 60 GHz. The transmitter antenna was a 2×2 microstrip patch array with a maximum gain of 10 dBi (see Section IV-A for the radiation pattern of the antenna) and the input power to the antenna was 2 dBm. An isotropic antenna was used as the receiver. Fig. 2(b)

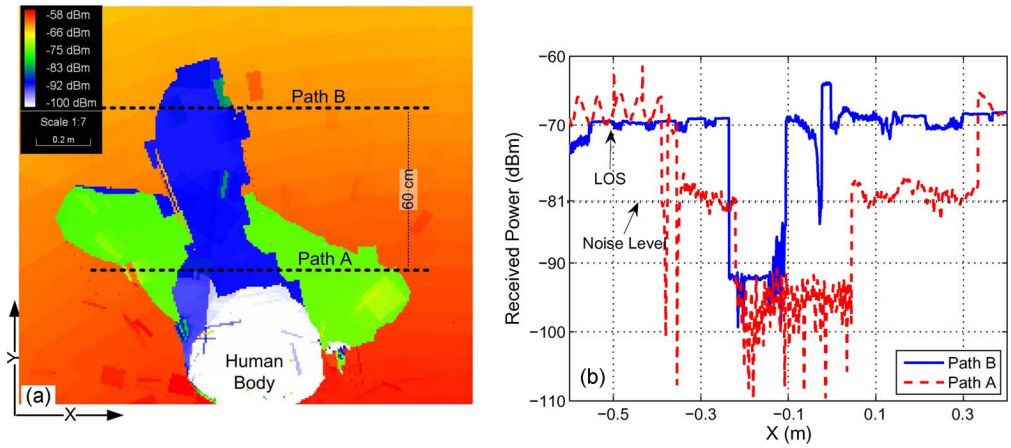

Fig. 2. (a) Received power over the rectangular grid in Fig. 1(b) around the human body. (b) Received power on Path A and Path B shown in Fig. 1(b).

shows the received power on two horizontal lines, named *Path A* and *Path B*, in the region shown in Fig. 2(a). Path A and Path B are respectively 20 cm and 80 cm in front of the human body and 1.7 m and 2.3 m away from the projected transmitter position in Fig. 1(b). The shadowing effect attenuates the received power level by 10 to 40 dB for Path A and by 15 to 30 dB for Path B. The other objects in the room cause up to ± 5 dB fluctuations in the received signal level. In calculating the received power the time-delay and phase of all rays, which their magnitudes are above -120 dBm, have been considered. This threshold is almost 40 dB below the thermal noise power with 2.16 GHz equivalent bandwidth.

B. Measurements

Fig. 3(a) demonstrates the developed test set-up to measure the shadowing loss of human body over the frequency range of 50–75 GHz. Two rectangular horn antennas with 24 dBi gain at 60 GHz and 10° beamwidth were used as the transmitter (Tx) and receiver (Rx). Agilent $E8267D$ programmable signal generator connected to $E8257DS15$ MMW source module was used to generate source signal. On the receiver side, Agilent $E4448A$ spectrum analyzer connected to $11974V$ preselected mixer was used to measure the spectrum of the received signal. The transmitted power was around 12 dBm. Wave absorbers with 40 dB attenuation were used to weaken the reflections from the source module and mixer. The Tx and Rx antennas were installed at the height of 135 cm and 130 cm, respectively. The horizontal distance between the Tx and Rx antennas in Fig. 3(b) was 3 m. The Tx antenna was fixed, but the Rx antenna was moved along a horizontal line in steps of 5 cm (the orientation of the Rx antenna was kept unchanged). At each point the received power spectrum was measured (after calibration) at three frequencies, i.e. 57, 60 and 64 GHz. For each spectral measurement, the average of 100 successive frames was taken to smooth the instantaneous fluctuations. Fig. 3(c) shows the LOS (no shadowing) measured spectrum at one of these Rx locations. It is seen that the measured power level reduces as the frequency increases, due to the larger path loss at the higher frequencies.

Fig. 3(d) compares the measured shadowing loss with ray-racing results for the same room. There is a good agreement between simulation and measurement from $x = -20$ to $x = 60$ cm. The maximum shadowing loss is around 40 dB which occurs when the human body blocks the LOS path completely. Ray-tracing results show that at deep shadowing region all LOS rays are absorbed by the human body, so the measured received power is the combination of NLOS rays. This result has been verified by the measurements in Fig. 3(d). A phased array receiver, as will be discussed in Section V-C, has the potential of steering the array beam to the direction of the strongest NLOS ray when the receiver is inside the deep shadowing region. Table II shows the range of parameters used in the link budget design of a MMW wireless network which uses CMOS phased arrays at its front ends.

III. Proposed 60 GHz Phased Array Transceiver Architecture

To steer the main beam of the phased array antenna, phase shifters can be incorporated in different stages of a receiver or transmitter. Hence, different phased array configurations have been developed. These configurations, which are shown in Fig. 4, are known as RF phase-shifting [22], Local Oscillator (LO) phase-shifting [23], IF phase shifting [24] and digital beamforming phased arrays [25].

In the RF phase shifting architecture, depicted in Fig. 4(a), different RF paths are phase shifted and then combined at RF frequency. The combined signal is then down-converted to the IF or baseband. In this architecture the spatial filtering of the strong undesired signals is performed at the combination point prior to the mixer. Hence, the upper dynamic range requirement of the mixer is relaxed and the level of unwanted in-band inter-modulations after mixer decreases. The design of the phase shifter on silicon, however, remains a challenge in this architecture. In addition, the insertion loss variation with phase shift should be small; otherwise, the array factor is deteriorated [26].

LO phase shifting architecture is displayed in Fig. 4(b). The main advantage of this architecture over RF phase shifting is that the phase shifter loss, non-linearity, and noise performance do not directly affect the receiver performance. However, as compared with the RF phase-shifting architecture, the number of components is larger. This leads to more silicon chip area and therefore higher cost. Besides, since the combining of signals

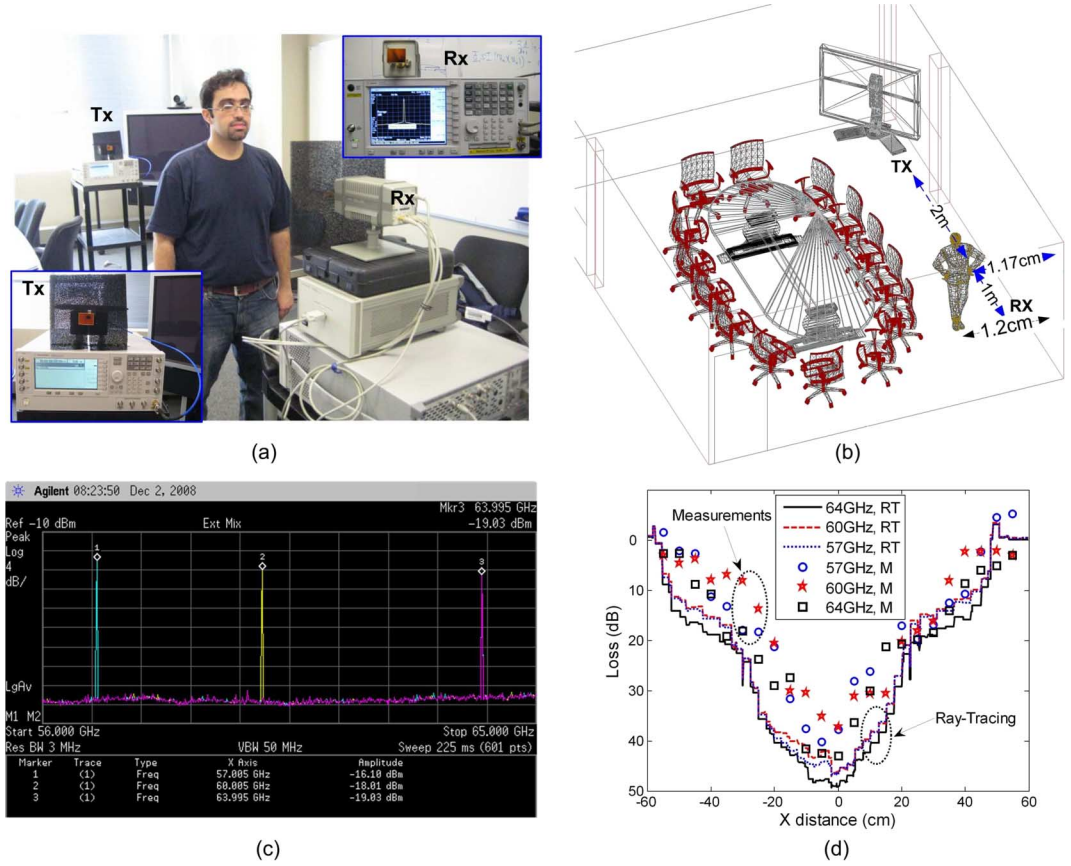

Fig. 3. Measurement environment and results. (a) Test set-up with transmitter and receiver. (b) Tx and Rx antenna locations in the room. (c) One sample of the measured spectrum at 57, 60 and 64 GHz. (d) Comparison of the measured and simulation results.

TABLE II
LINK-BUDGET DESIGN FOR A 60 GHz WIRELESS NETWORK USING CMOS TECHNOLOGY

Link Parameter	Range
Coverage Range	$\leq$ 10 m
Frequency	57-64 GHz
Bandwidth	$\geq$ 2.16 GHz
Bit Rate	$2-4$ Gb/s
Maximum LOS Loss	88 dB
Shadowing (Multipath) Loss	20-40 dB
P_T Power Amplifier	$\leq$ 2 dBm
Thermal Noise (B=2.16GHz, $T_0 = 290^{\circ K}$)	-81 dBm
LNA Gain	$\leq$ 25 dB
Receiver Noise Figure	6-10 dB
Rx Antenna Element Gain	$\geq$ 7 dBi
Tx Antenna Element Gain	$\geq$ 7 dBi
Array Beam Coverage	$\geq \pm 60^{\circ}$
Number of Antenna Elements	9 or 16

and beamforming are performed after mixers, in-band intermodulations are stronger. Also the upper dynamic range of the mixer must be high enough to stand strong interference signals.

Fig. 4(c) shows the IF phase shifting architecture. The phase shifters are placed at the first IF stage. The phase-shifted IF signals are combined before downconversion to baseband. As compared to RF phase shifting architecture, some of the challenges in phase shifter design are relaxed. However, since it needs multiple mixers, this architecture is not a proper option for low cost and low power phased array transceiver. Fig. 4(d) illustrates digital array architecture. Down-converted to a suitable IF frequency, each RF path is digitized by an analog-to-digital converter (ADC) and all outputs are passed to a digital signal processing (DSP) unit, which executes all tasks of beamforming and recovering the desired signal from the undesired interferences. The dynamic ranges of mixers and ADCs must be high enough to withstand the probable strong interferences. In case of WPAN since the data rate may exceed 2 Gb/s, very high-speed ADC's are required and to accommodate the required dynamic range each ADC must have a large number of bits which increases the ADC cost and power consumption extensively.

Table III summarizes the comparison of different phased array architectures in terms of power consumption, chip area and design challenges. To overcome the high path loss and shadowing loss at 60 GHz as well as CMOS output power and noise figure limitations multiple antennas and phase shifters are required. Considering Table III, the most appropriate configuration to lower the cost and power consumption and achieve a compact CMOS phased array transceiver is the RF phase shifting architecture. However, designing an efficient front-end as well as developing fast, efficient beamforming algorithms are the keys to overcome the phase shifter non-idealities and challenges in RF path. Fig. 5 demonstrates the proposed block diagram of an RF phase shifting 60 GHz phased array trans-

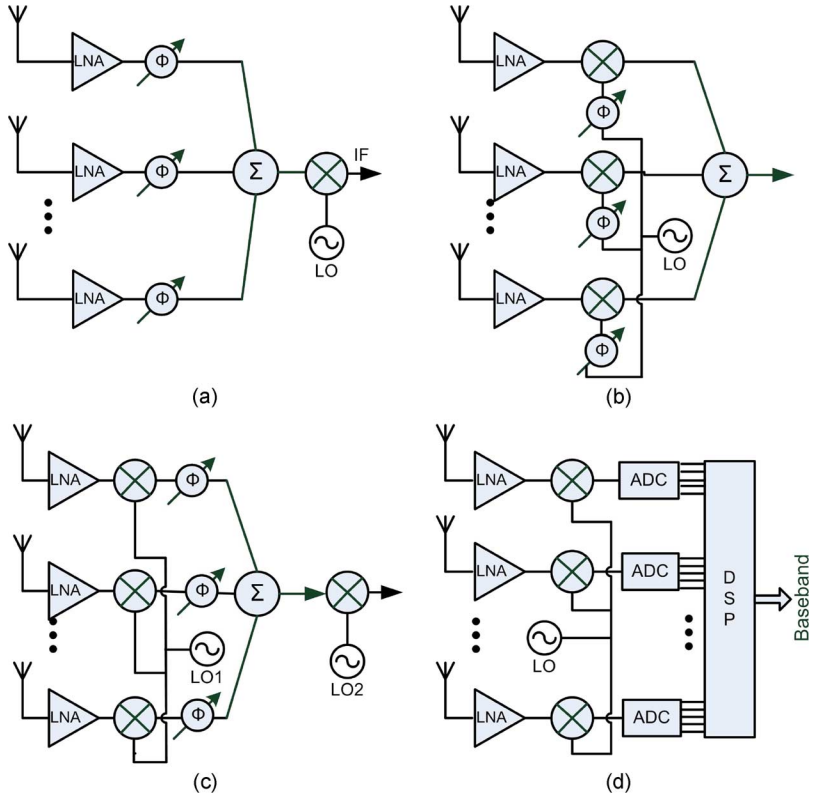

Fig. 4. Different phased array configurations (a) RF phase shifting, (b) LO phase shifting (c) IF phase shifting, and (d) digital beamforming array.

TABLE III
OVERALL COMPARISON OF DIFFERENT PHASED ARRAY ARCHITECTURES

Architecture	Power Consumption	Chip Area / Cost	Design Challenge
RF Phase-Shifting	Low	Low	Efficient front-end / Phase Shifter / Beamforming Algorithm
LO Phase-Shifting	High	High	Linearity / LO distribution / Coupling
IF Phase-Shifting	High	High	Linearity / LO distribution
Digital Array	High	High	Linearity / High dynamic range, fast ADC

ceiver. The receiver has a dual conversion architecture. The first mixer downconverts the combined RF signal to the first IF of about 8 GHz and the second I and Q down-conversion transforms the IF signal directly to the baseband. The image of the first down-conversion is 16 GHz far from the desired signal and can be easily rejected by an on-chip band pass filter before the first down-conversion. The analog baseband signal is amplified and after filtering is converted to a digital signal by two high speed A/D converters in I and Q channels. A fraction of the IF signal goes to a power detector and provides an estimate of the power level for the beamforming algorithm. The algorithm which will be described in Section V adjusts the phase shifters (and gain of each LNA if required).

In the transmit section, both I and Q digital signals are converted to analog domain by two high speed D/A converters. Harmonics of converted signals and spurious signals are rejected by two low pass filters. The filtered signal is then up-converted to the 8 GHz IF by the first I and Q up-conversion stage. The LO feed-through at the first up-conversion stage is minimized by calibration techniques implemented in the DSP. After another stage of filtering and amplification the signal is up-converted to 60 GHz. LO feed-through and generated spurious at the output of the second mixer are filtered out by the band pass filter centered at 60 GHz. The 60 GHz signal is then divided and applied to a number of paths. The signal in each path passes through a

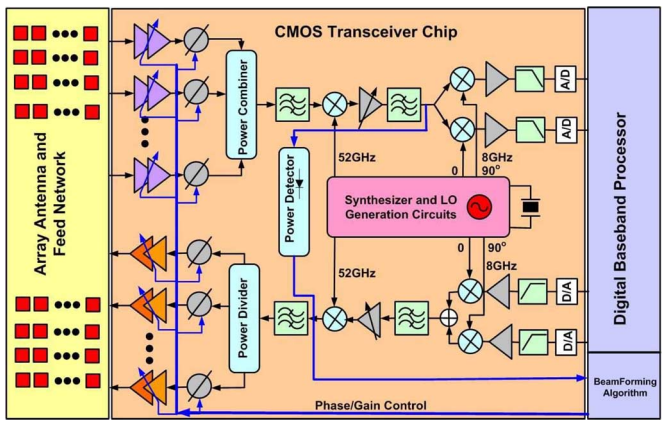

Fig. 5. Block diagram of the proposed RF phase shifting phased array transceiver at 60 GHz band.

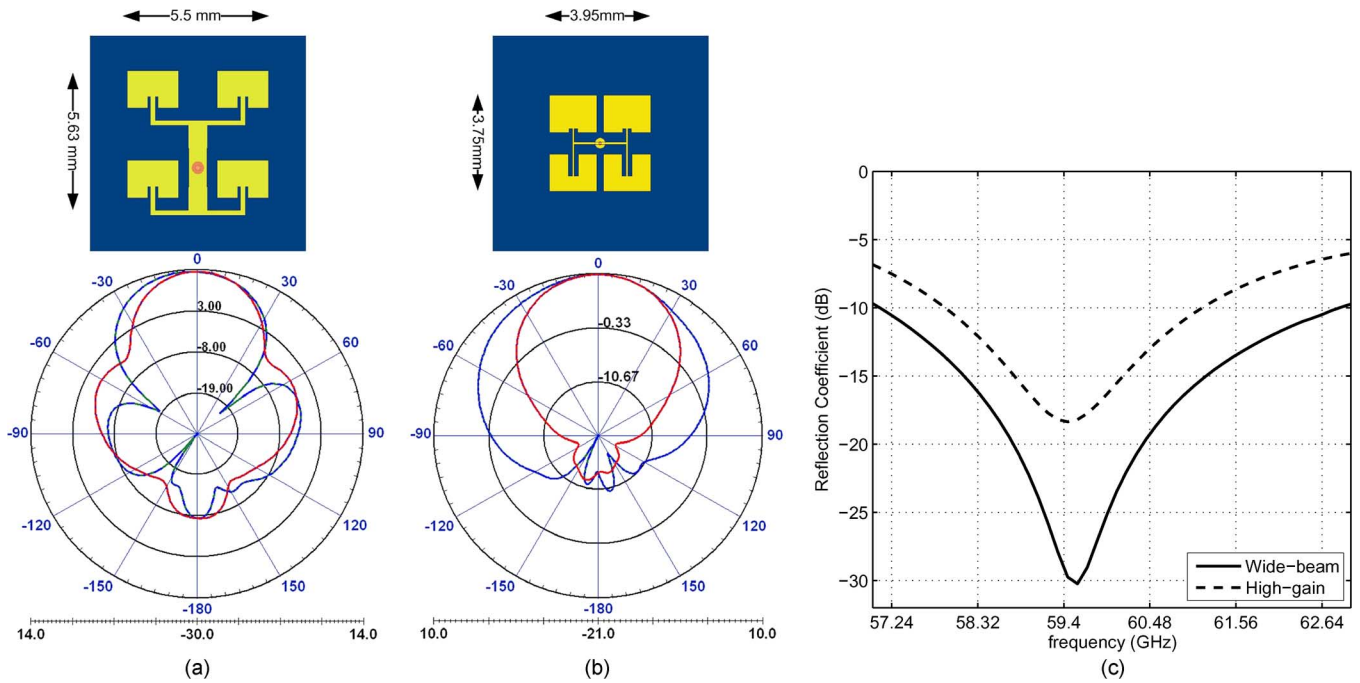

Fig. 6. Configuration and radiation pattern of two designs for 2 × 2 patch arrays. (a) The maximum gain design. (b) The maximum beamwidth design. (c) Reflection coefficients of the patch arrays.

phase shifter block. The phase shifted signals are then amplified by power amplifier (PA) stages and applied to the transmit antenna array. The saturated output power of a 90 nm CMOS PA is around 10 dBm but to accommodate sufficient linearity for the complex amplitude sensitive modulations such as QAM, the output power of power amplifier is set to 2 dBm to keep the PA in its linear operation region.

IV. Design and Measurement of 60 GHz Phased Array Components

In this section the design and analysis of the key components of a 60 GHz phased array receiver, namely antenna element, LNA and phase shifter, are described, and measured results for LNA and phase shifter are presented.

A. Off-Chip Wide-Beam Antenna Design

A substantial body of research on millimeter-wave antenna has been conducted [2], [27]–[30]. For fixed wireless access (FWA) applications, a high gain antenna is preferred to relax the performance requirements of the front-end elements. A high gain antenna has a narrow beam. Thus, for mobile applications, where a wide antenna coverage is required (see Table II), a single high-gain antenna is not an appropriate choice. For MMW wireless networking applications ($R_{max} < 10$ m), assuming the base station has been located at the center of the ceiling, almost 2.5 m above the user, the antenna beam coverage should be greater than $\pm 65^\circ$ to cover the whole area of a room or office. A wide beam coverage and a high radiation gain cannot be achieved at the same time unless a *phased array antenna* with beam steering capability is used. Even in this case the 3 dB beamwidth of each array element must be more than 65° to limit the beam steering loss. For this beamwidth the element gain is limited to 10.2 dBi [31]. Thus, designing the appropriate antenna element for 60 GHz WPAN is a delicate task.

A single rectangle patch antenna which is excited by its fundamental mode (TM10) has about 7 dBi gain and more than 100° beamwidth [32]. Patch antenna is considered as a planar radiator that can be integrated easily with the rest of the system; hence, it is widely used for wireless applications. To obtain higher gains one can use an array of the patches. In this section, two different 2 × 2 arrays of patch antennas are designed and compared. The first antenna is designed for the maximum gain and the second one for the maximum beamwidth. A very low loss substrate (RT/duroid −5880) is chosen with $\tan\delta = 0.0009$. Fig. 6 shows the structure of both antennas.

In the first design, the patches are placed about 0.7λ far from each other. The overall gain of the 2 × 2 array is 13.1 dBi, and the HPBW of the structure is only 36°. In the second design, the gain is scarified by 3 dB to achieve a wider beamwidth. The gain of the second structure is 10.1 dBi while the HPBW is 65°. Fig. 6 also shows the polar plot of the gain of both structures for both E-plane and H-plane. Further analysis shows that the radiation efficiency of the wide-beam antenna excluding the matching network, is around 90% over the frequency range of 57–63 GHz. Such high values for efficiency have been reported for MMW antennas before [33].

B. Optimum Low Noise Amplifier Design

Recently, different CMOS topologies which are mostly inspired by low frequency designs are utilized and implemented at 60 GHz band such as common-gate [34], common-source [35] and cascode [5], [36]. Compared to the common-gate (CG) or common-source (CS) topologies, the cascode topology shows a better isolation and higher gain. Although the noise figure of cascode configuration might be larger than that of CC and CB,

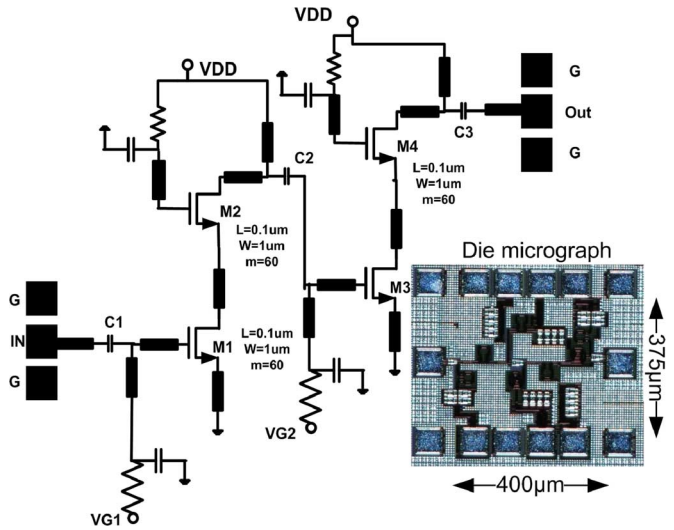

Fig. 7. The designed two-stage cascade amplifier and the die micrograph of the realized high gain LNA at 60 GHz band in 90 nm CMOS technology.

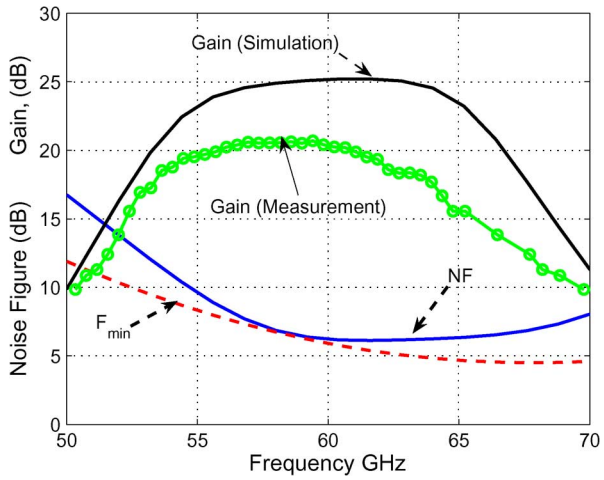

Fig. 8. Noise figure and gain of the designed LNA versus frequency.

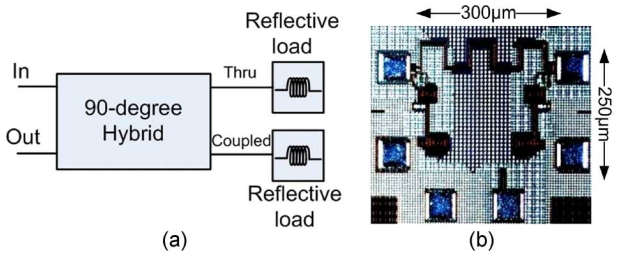

Fig. 9. (a) General block diagram of the reflective-type phase shifter. (b) Die micrograph of the fabricated analog phase shifter in 90 nm CMOS technology.

but its larger gain lowers the total noise figure of the system. Fig. 7 depicts the schematic of a two-stage amplifier using the proposed cascode amplifier design. It consists of a cascode topology with lumped inductors or inductive transmission lines in the source of the lower transistor, gate of the upper transistor and in between the two transistors. Also biasing of drain and gate has been provided through the lumped elements that are part of the matching circuit. The MOS transistors for the LNA are sized for maximum available gain in 90 nm-CMOS technology with a 1 V supply voltage. The device size is $60\ \mu\mathrm{m}/0.1\ \mu\mathrm{m}$. Each cascode stage consumes about 9 mA, so the total dissipated power is about 18 mW. All the lumped inductors and interconnectors for biasing, interconnecting and matching are simulated and optimized in ADS. Furthermore, ADS Momentum is utilized to model the interaction between inductors, T-junctions, bends and transmission lines. For the transistor, the RF model provided by foundry (STM) is used. Optimum cascode LNA described in [37] was utilized to improve the LNA gain and reduce the noise figure. For the off-chip antenna case, pad and ribbon bonding parasitics were incorporated into the LNA input matching. Fig. 8 shows the simulated LNA gain and NF. About 25 dB gain is achieved in this design. Also, the minimum noise figure F_{min} is about 6.1 dB.

Measured LNA Gain: Fig. 8 also shows the measured gain of the two-stage LNA (fabricated in 90 nm CMOS technology) shown in Fig. 7. The maximum gain of the LNA is above 20 dB over the frequency range of 56 GHz to 61 GHz. This amount of gain is sufficient to diminish the noise generated by those stages of phased array receiver following the LNA. The difference between the simulated and measured values for LNA gain is due to the approximate transistor models at millimeter wave and extra loss in interconnects and matching elements.

C. Phase Shifter Design

The objectives of the phase shifter design are minimizing the insertion loss and its variation, and maximizing the phase linearity versus control voltage. The authors have reported a beamforming technique which compensates for the remaining insertion loss variation of the phase shifters [26].

In general, phase shifters can be classified into digital and analog types. Although, the linearity of digital phase shifter is fairly well, the loss associated with the switches is still a challenge [38]. Moreover, digital phase shifters do not provide continuous phase shifting, which causes high side-lobe level in the radiation pattern of the antenna, and beam pointing errors. In contrast, analog phase shifters vary the phase continuously. Two well-known analog structures for phase shifters are vector summing and reflective-type phase shifter (RTPS). The linearity of the vector summing phase shifter is limited due to the active phase shifting. Furthermore, a large amount of power must be consumed to achieve a high dynamic range [39], [40]. Hence, in this work the focus is placed on RTPS type to provide a continuous, low-power phase shift over the desired frequency band.

Fig. 9 shows the general block diagram of the RTPS, which employs a 4-port 90°-hybrid and two similar purely imaginary (reflective) loads. The through and coupled ports of the hybrid are terminated to the reflective loads and the isolated port is used as the output. The reflective loads are varied electronically by changing the control voltage. Thus, the phase of the reflection coefficient at the through and coupled ports changes, which results in the phase shift of the output signal. The amount of the phase shift depends on the load reactance. Several passive terminations are proposed for the reflective loads. A single varactor cannot provide a phase shift more than 75° in practice [41].

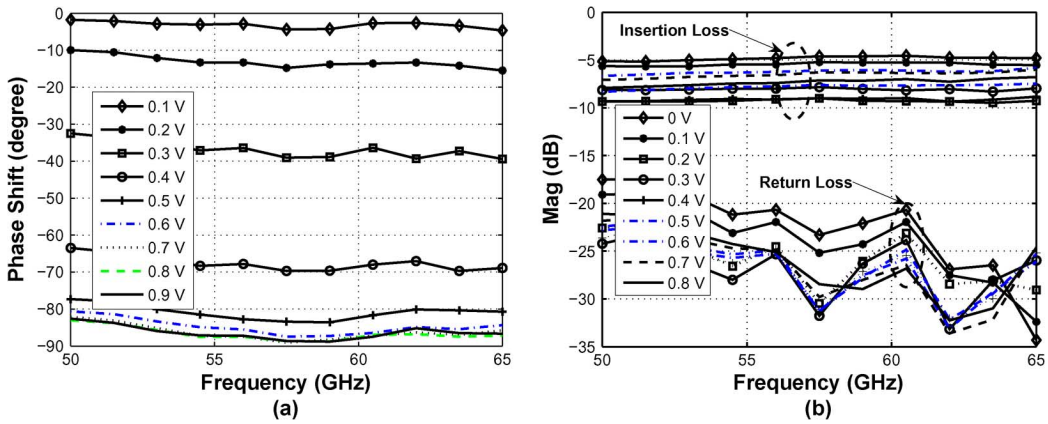

Fig. 10. Measured characteristics of the phase shifter over the frequency range of 50–65 GHz for the DC tuning voltage of 0–0.8 V, (a) phase shift. (b) Insertion loss (S_{12}) and return loss (S_{22}).

Adding a series inductor can increase the phase shift up to 180°. To achieve a complete 360° phase shift one should use dual resonant loads [41]. The RTPS, being fundamentally passive, shows linear input-output characteristics [42]. The main challenge in the integrated CMOS based RTPS design is the loss.

The main sources of loss in an RTPS are the transmission-line loss in the 90°-hybrid and the loss in the reflective terminations. To reduce phase shifter loss, active, negative resistance circuits have been used [43]. This, however, limits the linearity and noise performance of the RTPS. The insertion-loss variation can also be minimized by using an equalization resistance and modification of the 90°-hybrid [44].

In this work, an RTPS with dual resonant loads is designed in 90 nm CMOS. For a relative broadband 90 degree hybrid a broadside coupler is used. The broadside structure is implemented on the thick metal layers of the 90 nm CMOS process. The coupler has been meandered to have a compact size. The varactor is implemented in CMOS by using a regular CMOS transistor in which the Source and Drain terminals are connected. This structure is similar to a diode which can be biased reversely to generate a variable capacitance. Circuit simulation demonstrates that by varying the applied DC voltage from 0 to 1 V, a transistor with $W = 7\ \mu\text{m}$ and $L = 0.37\ \mu\text{m}$ can work as a varactor with a minimum capacitance of 49 fF and a tuning ratio of 3. The typical Q of the varactors in this technology is not higher than 10. The proposed reflective load consists of two inductors, a capacitor and the varactor. The die micrograph of the fabricated RTPS is depicted in Fig. 9(b). The area of this device is 0.35 mm × 0.2 mm which is smaller than other CMOS phase shifters in this band (see Table I in [42]). Fig. 10(a) and (b) depict the phase shift and insertion loss variation of the phase shifter over the frequency range of 50–65 GHz. When the input DC voltage is changed between 0 and 0.8 V, the phase shift changes from 0 to 90°. Furthermore, the measured insertion loss varies from 4.5 dB to 8 dB at 60 GHz.

By using parallel resonant loads, the maximum phase shift can be enhanced. Fig. 11(a) and (b) demonstrate the characteristics of the simulated RTPS with parallel resonant loads versus bias voltage for f = 58, 60 and 62 GHz. The phase sweep for $0.1\ \text{V} \leq v_B \leq 0.65\ \text{V}$ is more than 370° for the whole frequency range. The maximum insertion loss variation is 2.75 dB, which occurs at the lowest frequency.

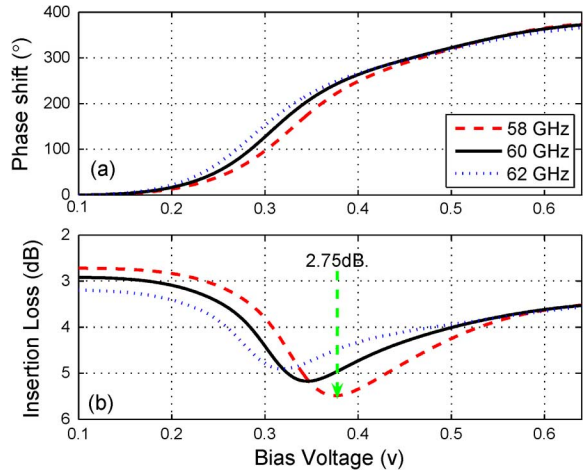

Fig. 11. Simulated phase shift and insertion loss of the designed phase shifter for 360° phase shift.

TABLE IV
SUMMARY OF THE PARAMETERS USED IN NOISE FIGURE CALCULATIONS

Design	η	LNA Gain	F_{LNA}	L_f	NF_{Tot}
90nm-CMOS	$\geq 90\%$	18–25 dB	5–7 dB	1–3 dB	6–10 dB

D. Noise Figure of the Phased Array Receiver

If the LNA gain is sufficiently high ($g \gg 1$), the system noise temperature simplifies to

$$T \simeq \eta T_i + T_0(L_f F_{LNA} - \eta) \tag{1}$$

where η, L_f, and F_{LNA} denote the antenna efficiency, front end loss, and noise figure of the LNA, respectively. Assuming the antenna temperature is equal to the room temperature ($T_i = T_0 = 290°\ \text{K}$), noise figure of the designed CMOS phased array receiver is between 6 to 10 dB as shown in Table IV.

V. Beamforming

In this section, two novel beamforming algorithms for the MMW receiver phased array antenna are proposed, and the achieved improvement in the signal to noise ratio at the array output is presented.

A. Beamforming Algorithms for MMW Receiver Phased Array

The goal of the beamforming algorithm is to increase the array factor and consequently provide the *SNR* determined by Bit Error Rate (BER) constrains. The ideal limit of the array factor is equal to the number of array elements; however, as it will be shown, the practical maximum array factor is smaller than that due to the variable insertion loss of phase shifter.

1) Signal Model: Let $\mathbf{X}(t) = [x_1(t)x_2(t)\cdots x_N(t)]$ denote the received signals by all elements of the array. Then it consists of three parts: source signal $\mathbf{x}_S(t)$, interference $\mathbf{x}_I(t)$, and background noise $\mathbf{n}(t)$,

$$\mathbf{x}(t) = \mathbf{x}_S(t) + \mathbf{x}_I(t) + \mathbf{n}(t). \tag{2}$$

The background noise is assumed to be spatially white. Assume the source (transmitter) is located at direction $\overrightarrow{\mathbf{r}} = (\theta_T, \phi_T)$ in the receiver array coordinate system, transmitting RF signals at frequency f_0. The RF signal received by an element of the array located at (x_n, y_n, z_n) is given by

$$x_s^n(t) = s_0(t)G_e(\overrightarrow{\mathbf{r}}) \times \exp\left[jk_0(x_n \sin\theta_T \cos\phi_T + y_n \sin\theta_T \sin\phi_T + z_n \cos\theta_T)\right] \tag{3}$$

where k_0, and $s_0(t)$ are respectively the RF wave number and the source waveform. The path loss is included in $s_0(t)$. The array output for a single receiver array structure shown in Fig. 4(a) is

$$y(t) = \mathbf{w}^H \mathbf{X}(t) \tag{4}$$

where $\mathbf{w}$ is the array weights vector and ^{H} denotes the Hermitian operator. If analog phase shifters, such as the one shown in Fig. 11, were used to adjust the array weights for beamforming the wight vector would be [45]

$$\mathbf{w}(v_1, v_2, \cdots v_N) = \left[f(v_1)e^{j\psi(v_1)}\ f(v_2)e^{j\psi(v_2)} \cdots f(v_N)e^{j\psi(v_N)}\right] \tag{5}$$

where v_i is the control voltage of the i^{th} phase shifter, and f and ψ denote the amplitude (insertion loss) and phase-shift functions of the phase shifter. The total received power by the array is then

$$P(t) = y^H y. \tag{6}$$

2) Statement of the Problem: In the absence of co-channel interference, beamforming for a MMW receiver array is a constrained optimization problem with the objective of maximizing the total received power by the array. The voltage dependent characteristics of the phase shifters form the constrains of the optimization problem. Hence, the beamforming problem can be stated as

$$\begin{aligned} &\text{maximize } P(w_1, w_2, \cdots, w_N) \\ &\text{subject to: } w_i = f(v_i)\exp(j\psi(v_i)) \\ &\qquad v_{\min} \le v_i \le v_{\max}. \end{aligned} \tag{7}$$

In [45], [46], the authors have shown that an efficient way to solve this problem is to use a gradient estimation approach such as zero-knowledge beamforming algorithm. In this case the control voltages are updated in an iterative manner

$$\mathbf{v}(n+1) = \mathbf{v}(n) + 2\mu\nabla_{\mathbf{v}}P(n) \tag{8}$$

where μ is an internal algorithm parameter called the *step size*, and $\nabla_{\mathbf{v}}P(n)$ is the gradient of power with respect to $\mathbf{v}$. Since the exact calculation of the gradient is not practical it is replaced by an estimated vector:

$$\nabla_{\mathbf{v}}P(n) \simeq [\hat{g_1}(n)\ \hat{g_2}(n)\ \cdots\ \hat{g_N}(n)] \tag{9}$$

where each component $\hat{g_k}(n)$ is the approximate partial derivative of $P(n)$ w.r.t. $v_k(n)$.

3) Reverse-Channel Aided Beamforming: The size and cost constrains of the 60 GHz receiver do not allow for incorporating a complex processor in the portable node. However, the access point (fixed node) can handle more elaborate signal processing tasks. Moreover, in MMW networking standards such as WPAN, 50 MHz of the spectrum is reserved for the reverse channel to carry the control signals between the access points and mobile nodes. Access point can be equipped with direction-of arrival (DOA) estimation unit. This unit can calculate the relative position of the mobile nodes and send this information to them. The mobile node can use this information to adjust its beam. Although this method is very fast, in the case of shadowing it is not efficient. In this case the beamformer must be able to maintain the array beam on the direction of the strongest component of the multipath signal.

B. Beamforming Results for LOS Propagation

Fig. 12 demonstrates the results of the *Aided Beamforming* algorithm for a typical case, where it is assumed that the equivalent noise bandwidth is 2.16 GHz, the receiver NF is 6 dB, the output power of the power amplifiers is 2 dBm, and the antenna element is the 2 × 2 patch array shown in Fig. 6(b). The 9-element phased array is a 3 × 3 square array with λ (5 mm) spacing. In Fig. 12 it is assumed that the user is moving away from the transmitter while both receiver and transmitter antenna axes are parallel. Fig. 12 compares the results of ideal, fast and slow beamforming for a 3 × 3 square array. Slow beamforming is the case where during one iteration of the algorithm user moves more than 1 cm, while in fast beamforming the user's displacement is less than 1 mm. The difference between ideal and fast beamforming when the user is close to the transmitting node

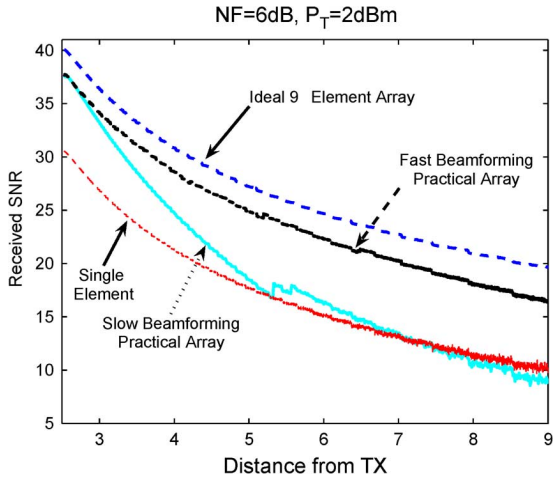

Fig. 12. Received SNR by a 3 × 3 square phased array antenna for different beamforming scenarios.

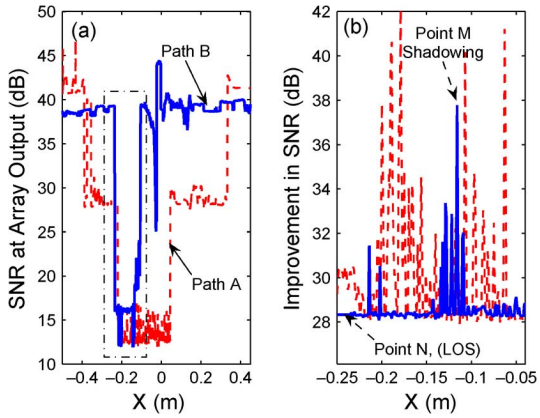

Fig. 13. Beamforming results for a 4 × 4 square array with λ spacing. The dashed and solid curves correspond to the receiver location on *Path A* and *Path B* in Fig. 2. (a) *SNR* at the array output after beamforming. (b) The improvement in *SNR* due to using phased array for the region shown by a rectangle in Fig. 13(a).

$(r \leq 3)$ m is 2 dB. As the distance increases to $r \geq 9$ m this difference raises to more than 3.5 dB.

Another important result of Fig. 12 is that the beamforming gain depends on the received power. So, as the distance between the portable receiver and the transmitting node increases, the performance of the beamforming degrades. Moreover, the beamforming speed affects the beamforming gain. A similar version of this algorithm has been successfully applied to a 34 element Ku-band phase array antenna [46]. The duration of each beamforming iteration was measured to be less than 5 ms with a 125 KHz Digital-to-Analog convertor.

C. Beamforming Results for NLOS Propagation

In this case, user location information is not available and the receiver seeks for the strongest signal by running a beam-search mode (acquisition phase). A method has been proposed for direction finding in [47]. Fig. 13 shows the results of beamforming with a 4 × 4 square array (with λ spacing), when the receiver moves along Path A and B shown in Fig. 2. When the receiver is close to the human body (Path A) the width of the fading region is larger ($x = -0.4$ m to $x = 0.35$ m) and the shadowing loss varies from 10 dB to 40 dB. Fig. 13(a) illustrates that the array output SNR is always above 12 dB. Fig. 13(b) shows the improvement in SNR after applying the proposed beamforming algorithm to a 16-element phased array. This improvement is due to three factors: using a 16-element array at the access point to increase the effective radiated power, using a 2 × 2 patch antenna element at the receiver (instead of an isotropic antenna), and the beamforming gain (array factor). While for the LOS section the improvement is 28 dB, it increases up to 42 dB in the shadowing region, implying that the proposed beamforming algorithm has an *excess gain* (up to 14 dB) when shadowing occurs. Increasing the number of elements in the array improves this gain.

Fig. 14 illustrates how the beamforming algorithm for NLOS propagation works. In this figure the strongest received rays for two receiver positions on Path B, namely *Point M* and *Point N* shown in Fig. 13(b), are depicted. Point M is in the deep shadowing region, hence its strongest ray has an excess delay of 21 ns and is 26 dB weaker than that of the point N. Fig. 14(b) and (c)

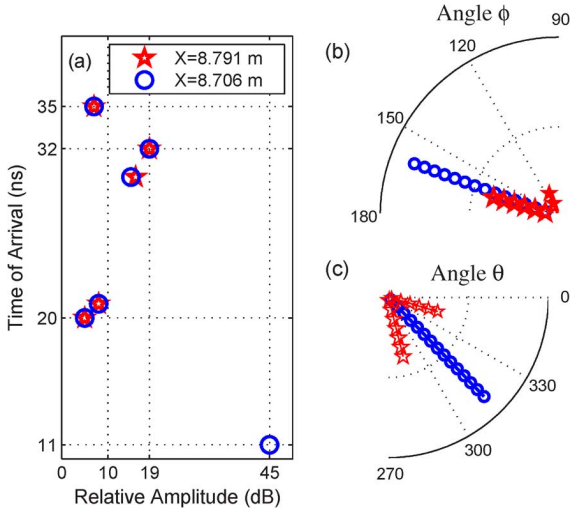

Fig. 14. Characteristics of the strongest received ray for two positions.

show the directions of the two strongest rays which are resolvable in their θ coordinates. If the signal level drops suddenly, the beamforming algorithm finds the strongest ray and steers the array beam to its direction.

VI. Conclusion

CMOS is the promising technology for low-cost high-volume 60 GHz transceivers. However, the fundamental limitations of current CMOS technology, such as low amplifier gain and output power as well as the fairly high noise figure restrict the performance of the single-antenna 60 GHz CMOS systems. It was shown that an adaptive (intelligent) integrated phased array antenna and radio system (at both ends) is the most viable approach to provide the required SNR for reliable MMW network operation. Moreover, the RF-phase shifting array configuration is a practical and low-cost architecture for 60 GHz applications. The efficiency of phased array system depends on the performance of LNA and phase shifter; hence, one objective of this paper was to present the design of a high-performance phase shifter and LNA in CMOS technology.

To design the link budget for 60 GHz network, the propagation of the MMW signal in an indoor environment was studied for LOS and NLOS scenarios, and verified by measurements. It was found that the shadowing loss of a human body can be as high as 40 dB. In this case all LOS rays are absorbed by the human body and only NLOS rays are received.

A low noise amplifier using cascode topology, was designed and fabricated in 90 nm CMOS technology. The measured gain of this two stage LNA exceeded 20 dB at the frequency range of 56–61 GHz. Furthermore, to meet the beamforming requirements, a broadband reflective type phase shifter in 90 nm CMOS with a linear phase and low insertion loss, was designed, fabricated and successfully tested.

Finally, a fast beamforming algorithm was developed to realize the potentials of phased array for both LOS and multipath signal propagation. The imbalanced insertion loss of phase shifters results in a margin between the ideal and practical array gain, which reduces the effective range or transmitted/received power by the array. Moreover, the beamforming gain is proportional to the input SNR. In the case of shadowing, the proposed beamforming algorithm seeks for the strongest ray. It was shown an excess gain up to 14 dB can be obtained by this method.

ACKNOWLEDGMENT

The authors would like to acknowledge CMC (Canadian Microelectronics Corporation) for device fabrication. The authors are thankful to Mr. J. Dietrich at CMC Advanced RF Lab at the University of Manitoba for on-wafer measurements, and Mr. H. Mirzaei.

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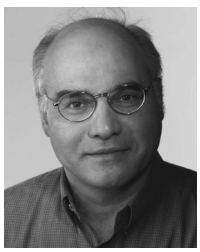

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