

VLSI Design

Lecture 19: Memory and Data path

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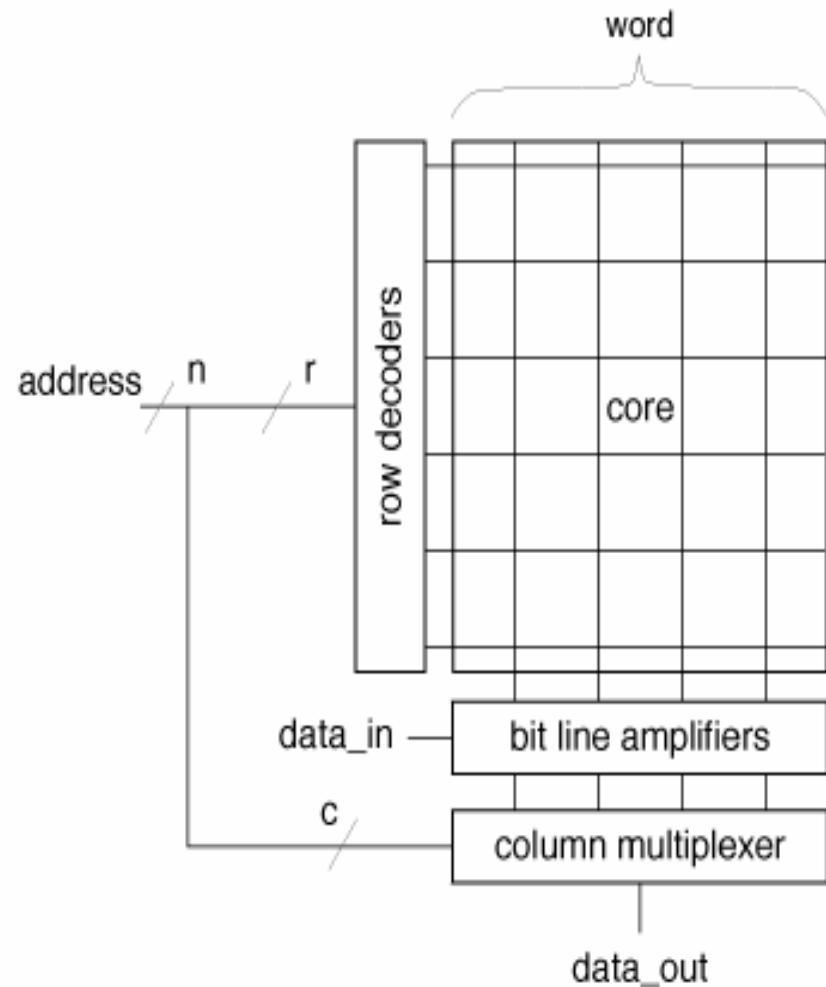
Adapted, with modifications, from lecture notes
prepared by the author (from Prentice Hall PTR)

Topics

- ❖ Memories:
 - ROM;
 - SRAM;
 - DRAM.
- ❖ Datapaths.
- ❖ PLAs.

High-density memory architecture

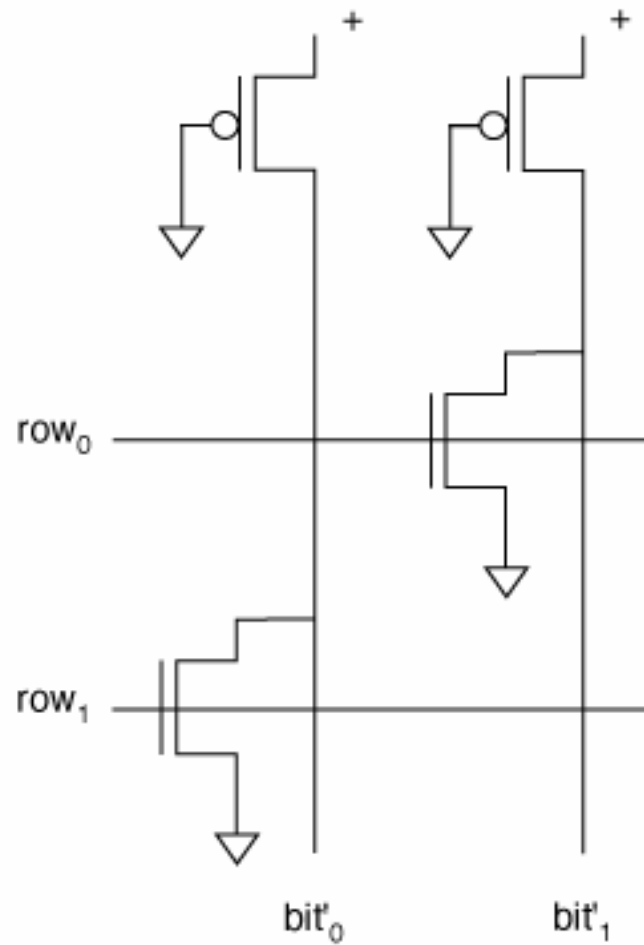
- ❖ Address is divided into row, column.
 - Row may contain full word or more than one word.
- ❖ Selected row drives/senses bit lines in columns.
- ❖ Amplifiers/drivers read/write bit lines.



Read-only memory (ROM)

- ❖ ROM core is organized as NOR gates
 - pulldown transistors of NOR determine programming.
- ❖ Erasable ROMs require special processing that is not typically available.
- ❖ ROMs on digital ICs are generally mask-programmed
 - placement of pulldowns determines ROM contents.

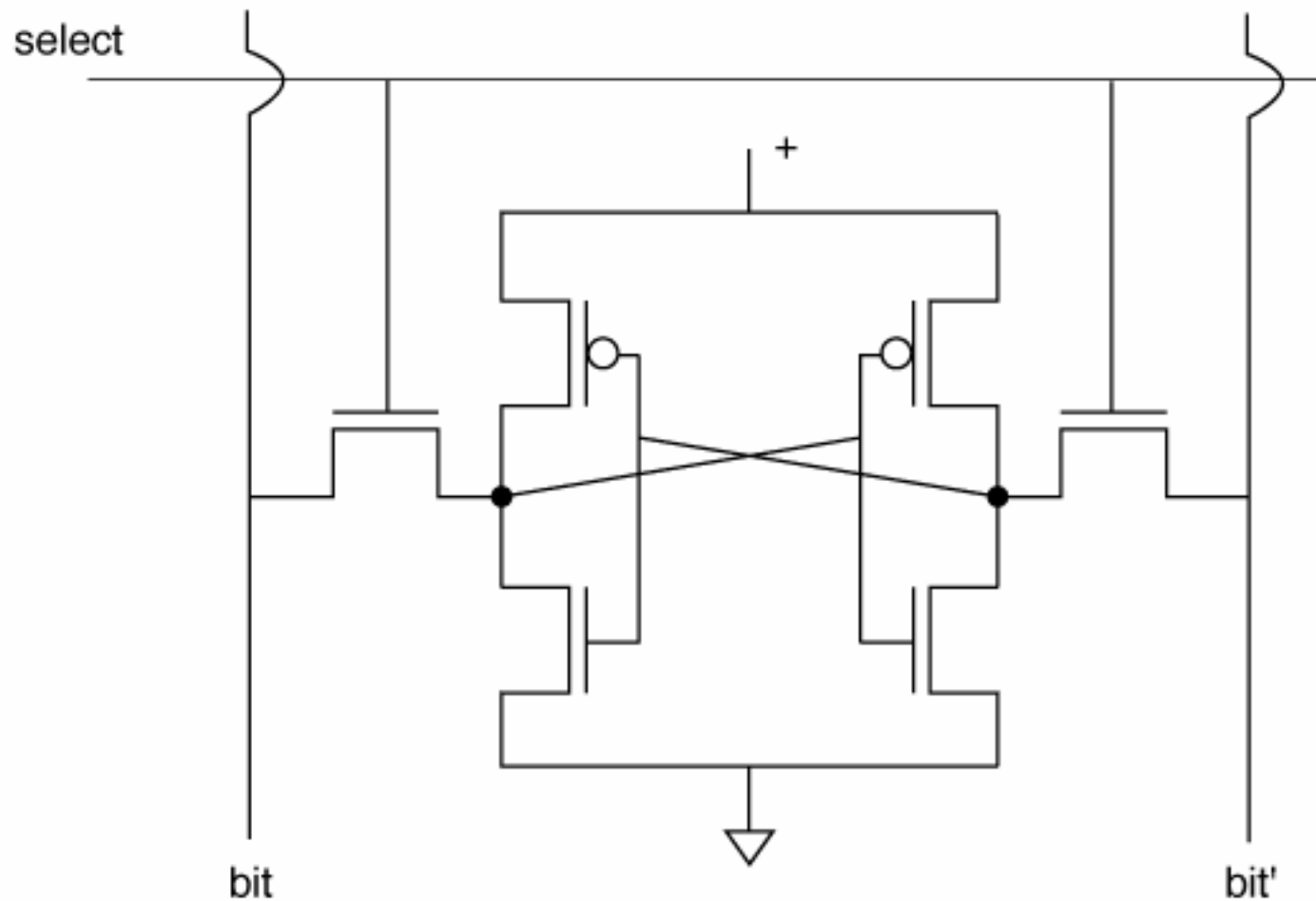
ROM core circuit



Static RAM (SRAM)

- ❖ Core cell uses six-transistor circuit to store value.
- ❖ Value is stored symmetrically: both true and complement are stored on cross-coupled transistors.
- ❖ SRAM retains value as long as power is applied to circuit.

SRAM core cell



SRAM core operation

❖ Read:

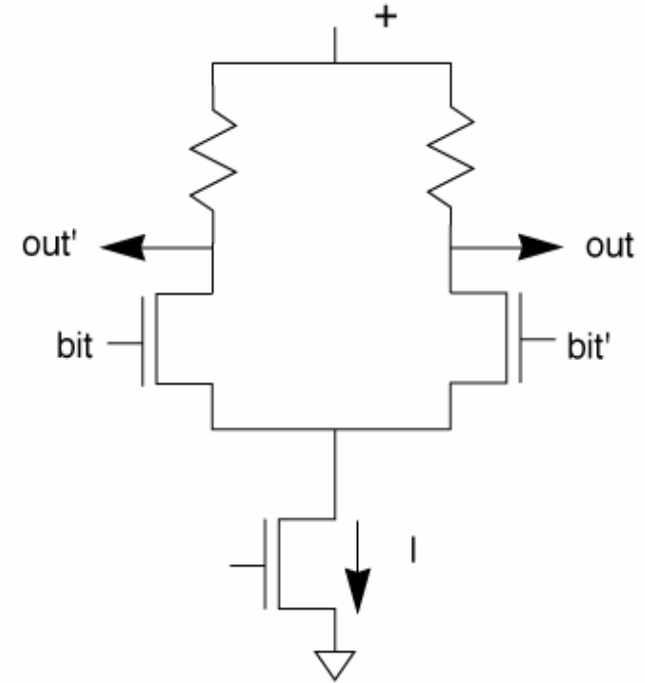
- precharge bit and bit' high (the two PMOS transistors for precharge not shown: source= V_{DD} , drain=bit/bit', gate=precharge');
- set select line high from row decoder;
- one bit line will be pulled down.

❖ Write:

- set bit/bit' to desired (complementary) values;
- set select line high;
- drive on bit lines will flip state (charge sharing) if necessary.

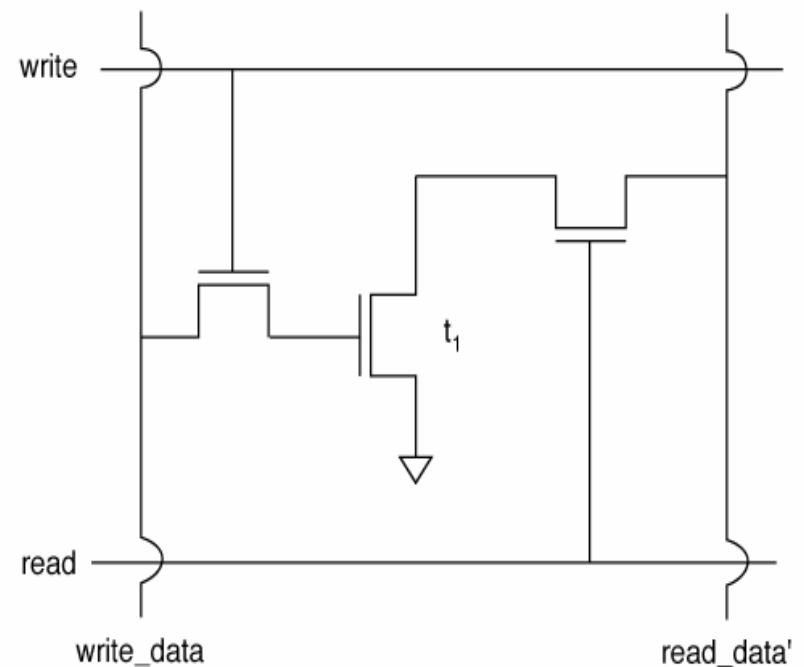
SRAM sense amplifier

- ❖ Differential pair: takes advantage of complementarity of bit lines.
- ❖ When one bit line goes low, that arm of differential pair reduces its current, causing compensating increase in current in other arm.
- ❖ Sense amplifier can be cross-coupled to increase speed.



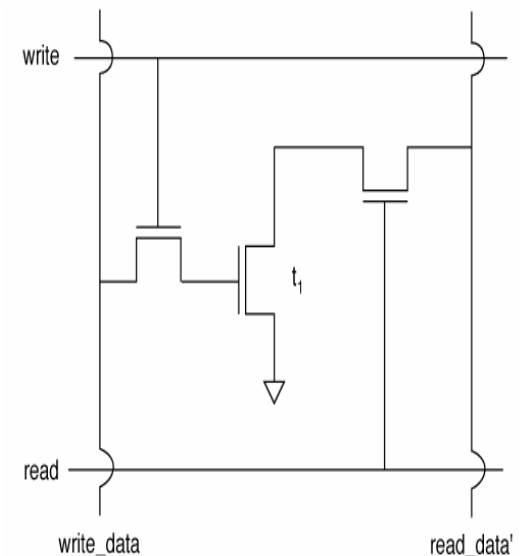
3-Transistor Dynamic RAM (DRAM)

- ❖ First form of DRAM
 - modern commercial DRAMs use one-transistor cell (requires poly-poly).
- ❖ 3-transistor cell can easily be made with a digital process.
- ❖ Dynamic RAM loses value due to charge leakage
 - must be refreshed.



3-T DRAM operation

- ❖ Value is stored on gate capacitance of t_1 .
- ❖ **Read:**
 - read = 1, write = 0, read_data' is precharged;
 - t_1 will pull down read_data' if 1 is stored.
- ❖ **Write:**
 - read = 0, write = 1, write_data = value;
 - guard transistor writes value onto gate capacitance.

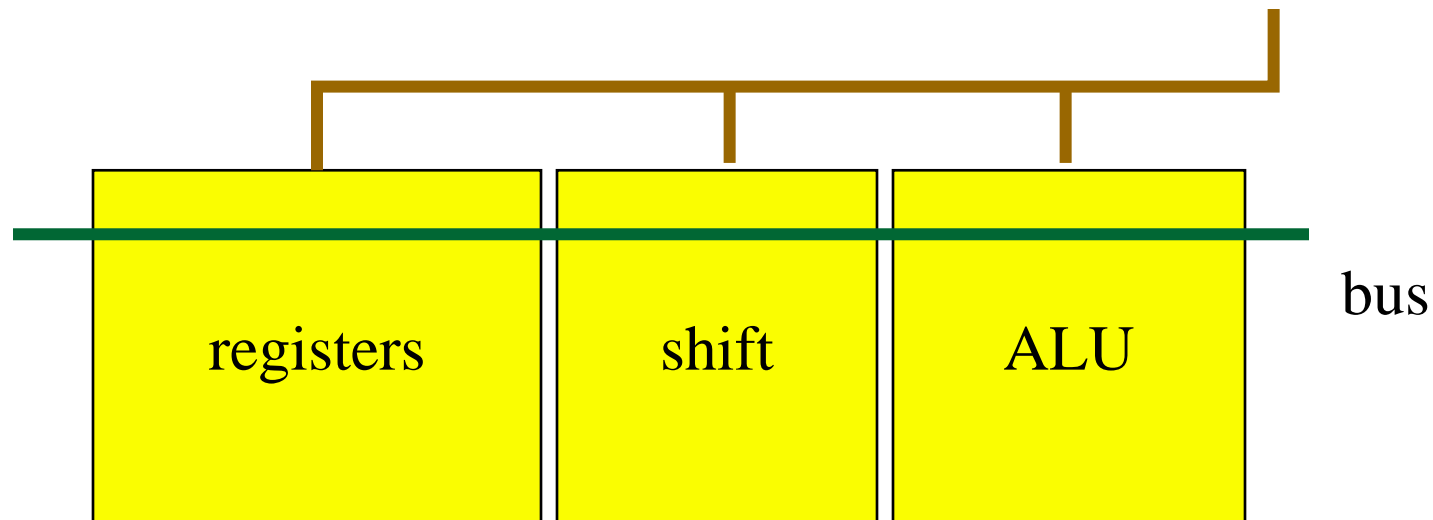


Data paths

- ❖ A data path is a logical and a physical structure:
 - bitwise logical organization;
 - bitwise physical design.
- ❖ Datapath often has ALU, registers, some other function units.
- ❖ Data is generally passed via busses.

Typical data path structure

Slice includes one bit of function units, connected by busses:

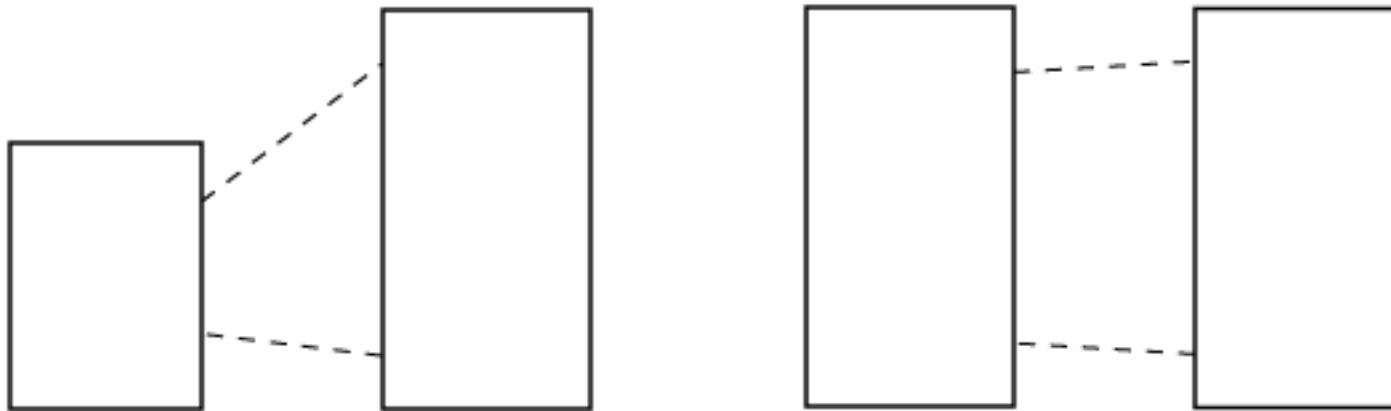


Bit-slice structure

- ❖ Many arithmetic and logical functions can be defined recursively on bits of word.
- ❖ A **bit-slice** is a one-bit (or n-bit) segment of an operation of minimum size to ensure regularity.
- ❖ Regular logical structure allows regular physical structure.

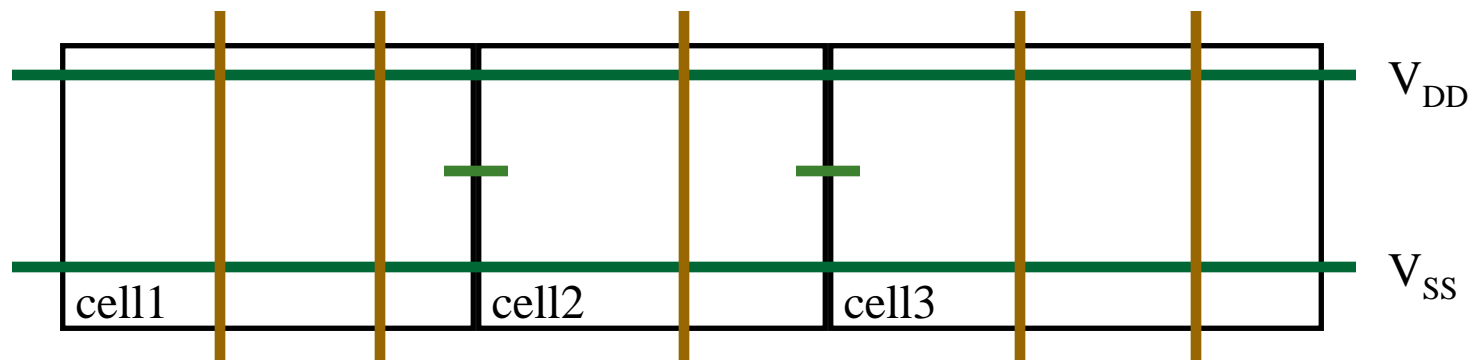
Abutting and pitch-matching

- ❖ Cells in bit-slice may be abutted together
 - requires matching positions on terminals.
- ❖ **Pitch-matching** is designing cells to ensure that pins are at proper positions for abutting.



Wiring plans

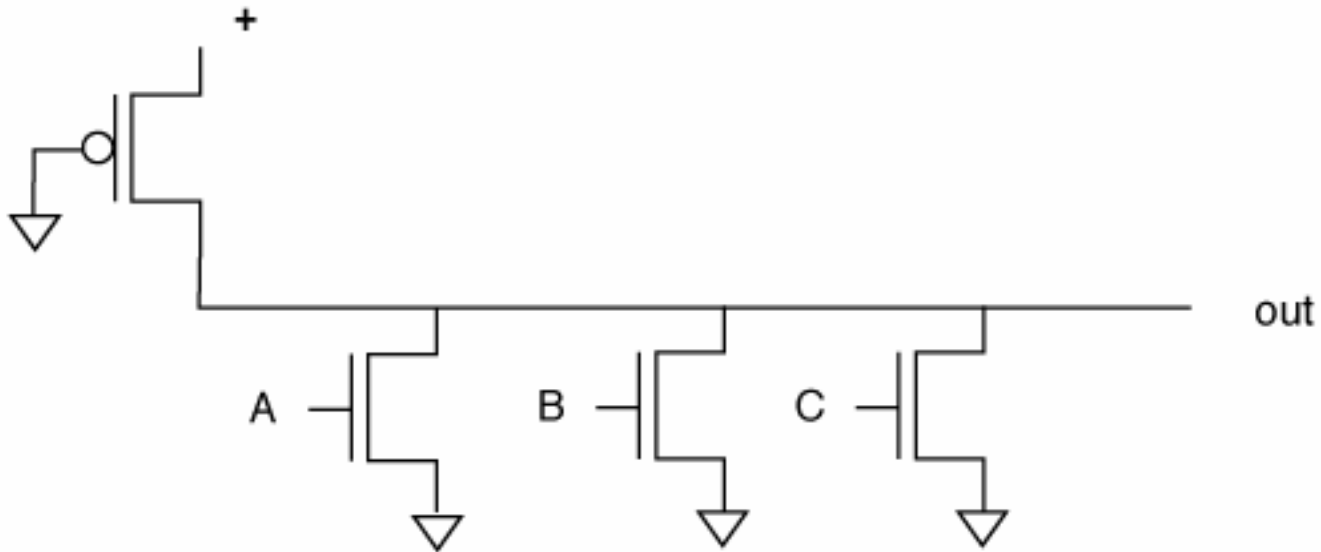
- ❖ A wiring plan shows layer assignments and directions for major signals.
- ❖ Put most important signals on lowest-impedance accessible layers.



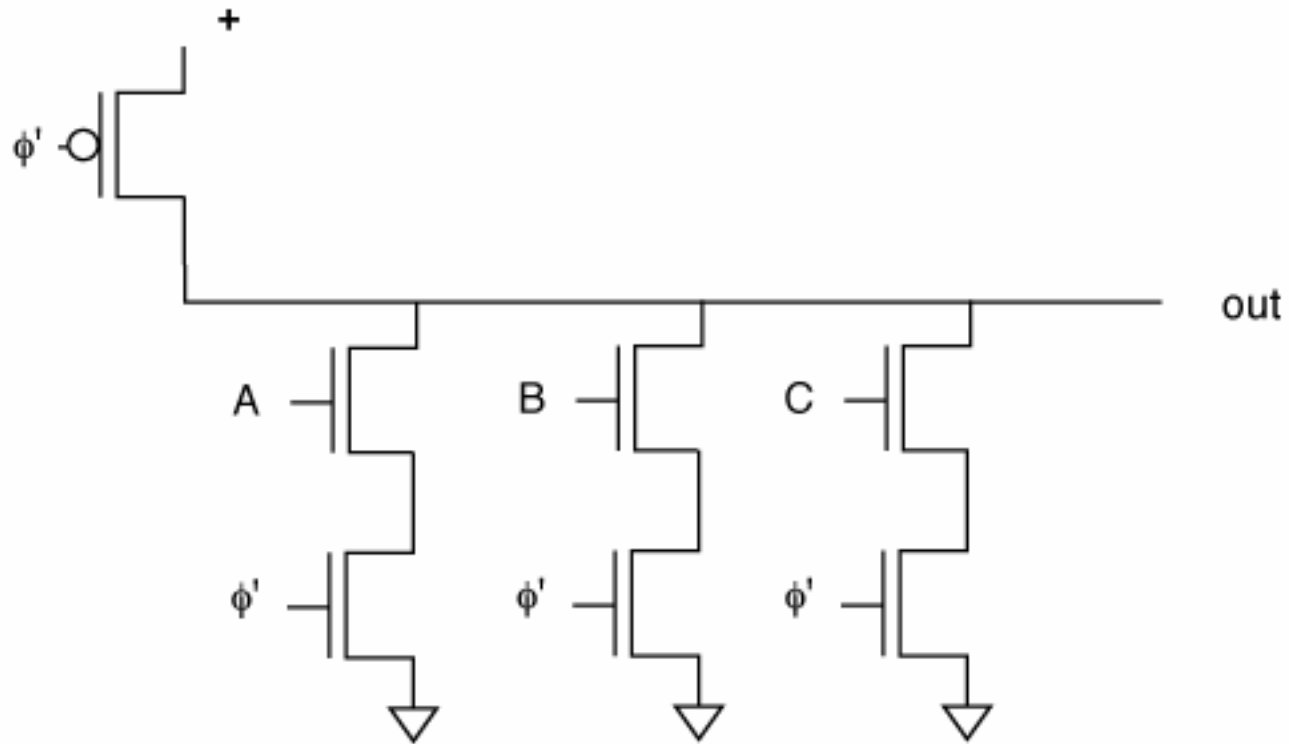
Bus circuits

- ❖ Cannot support full connectivity between all data path elements
 - must choose number of transfers per cycle allowed.
- ❖ A bus circuit is a specialized multiplexer circuit.
- ❖ Two major choices:
 - pseudo-nMOS,
 - precharged.

Pseudo-nMOS bus circuit



Precharged bus circuit

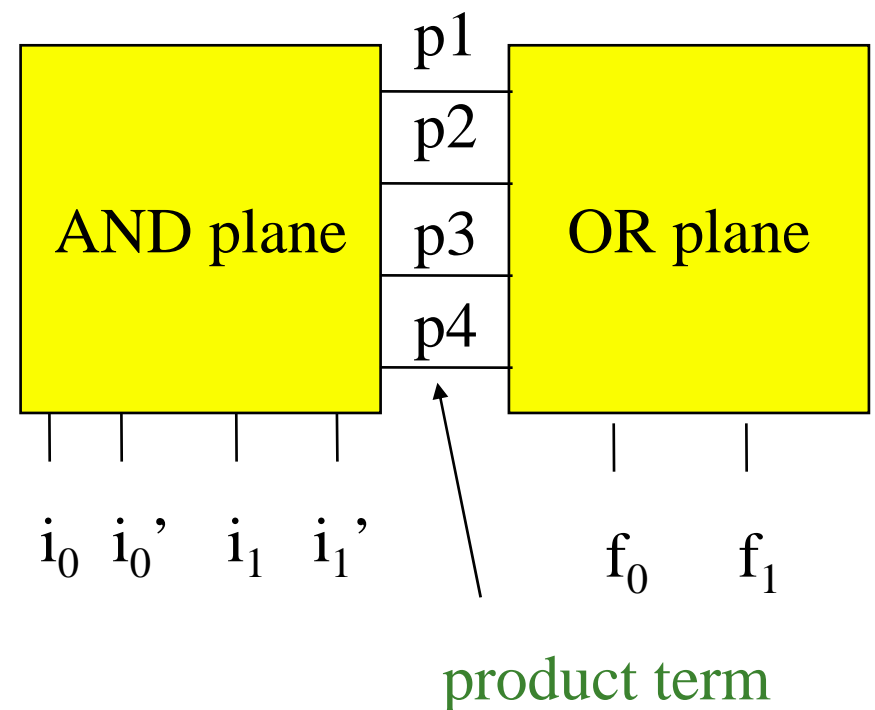


Programmable logic array (PLA)

- ❖ Used to implement specialized logic functions.
- ❖ A PLA decodes only some addresses (input values); a ROM decodes all addresses.
- ❖ PLA not as common in CMOS as in NMOS, but is used for some logic functions.

PLA organization and structure

- ❖ AND plane, OR plane, inverters together form complete two-level logic functions.
- ❖ Both AND and OR planes are implemented as NOR circuits.
- ❖ Pulldown transistors form programming (personality) of PLA. Transistors may be referred to as programming tabs.



PLA AND/OR cell

