

VLSI Design

Lecture 16: Sequential testing

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Sequential testing

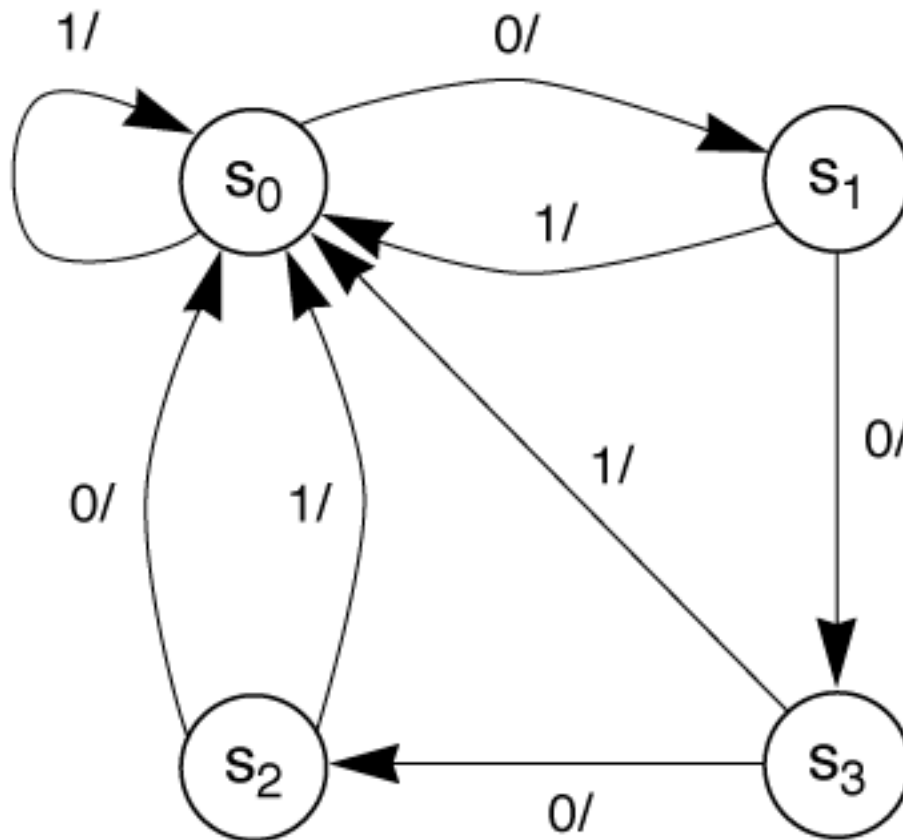
- **Much harder than combinational testing: can't set memory element values directly.**
- **Must apply sequences to put machine in proper state for test, be able to observe value of test.**

Testing the machine

(See the figure in the text book)

- **To test NAND for stuck-at-1, must set both NAND inputs to 1.**
- **Primary input i1 can be controlled directly.**
- **To set lower NAND input, must set state to $ps0 = ps1 = 1$.**

Example state machine



State codes:

$s_0 = 11$

$s_1 = 10$

$s_2 = 01$

$s_3 = 00$

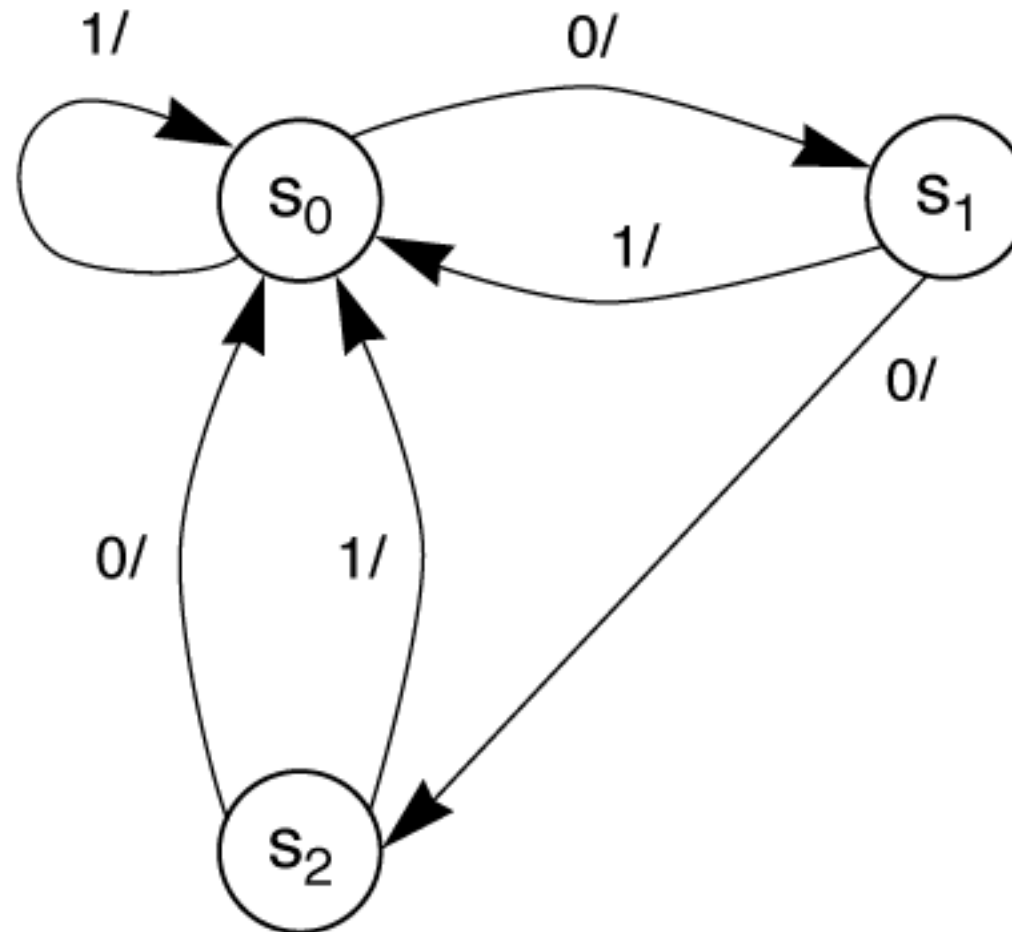
Controlling an FSM

- **Don't know initial state of machine.**
- **Must find a sequence which drives machine to required state, independent of initial state.**
- **State sequence for test:**
 - * **-> s0 -> s1 -> s3.**

Unreachable states

- **State assignment may cause some states to be unreachable.**
- **As a result, it may not be possible to apply some required test values.**

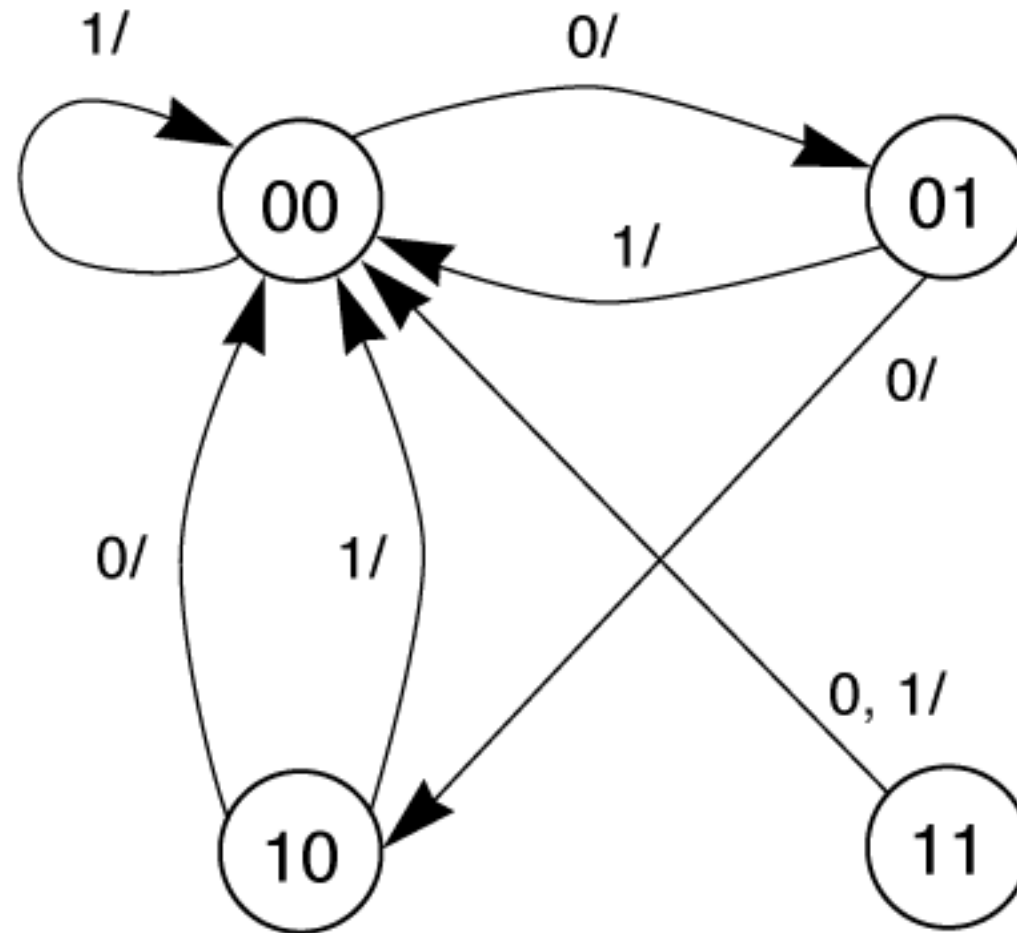
Unreachable state example



Example

- **State codes:**
 - **s0 = 00**
 - **s1 = 01**
 - **s2 = 10.**
- **This creates a fourth state which is unreachable.**

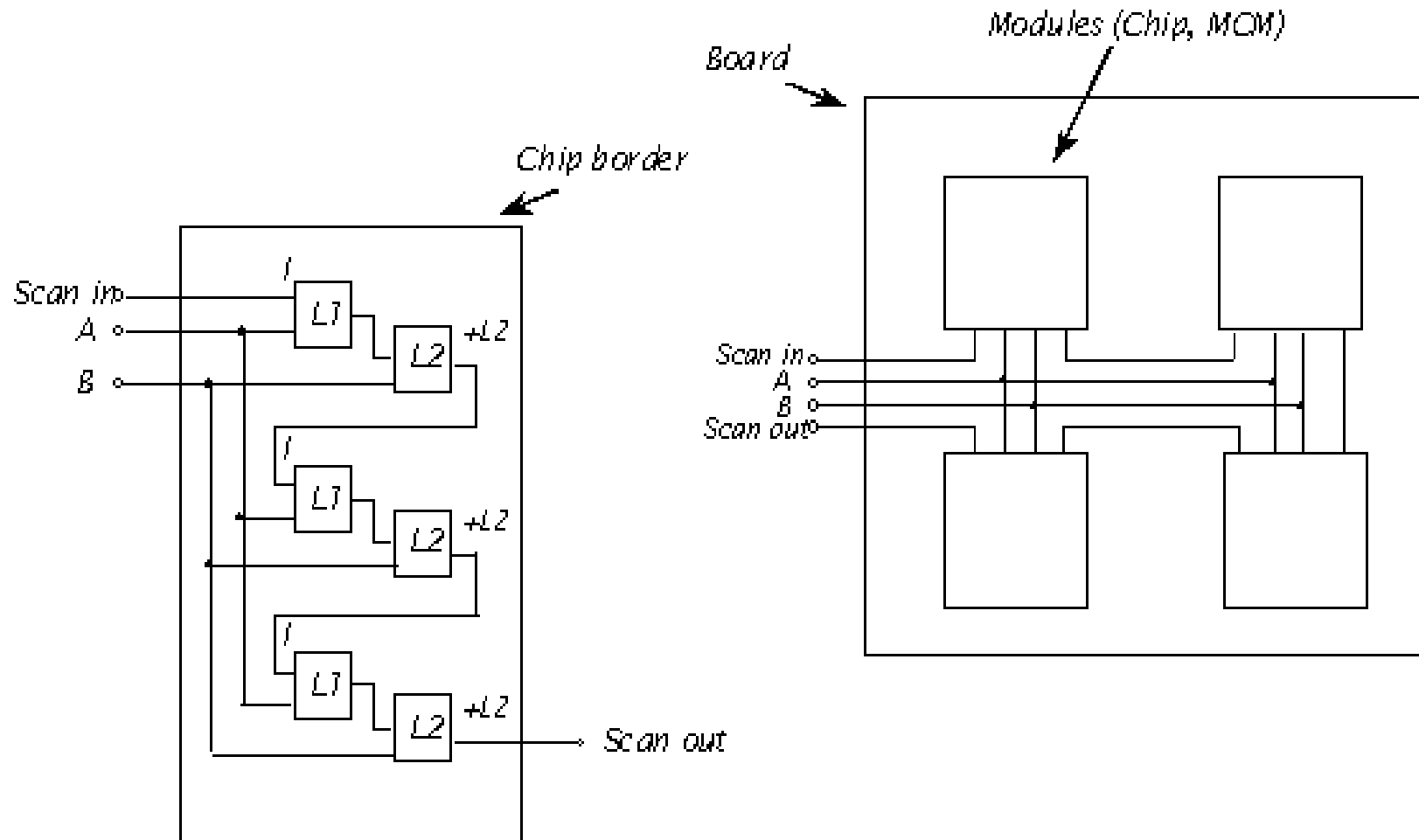
Implemented FSM



LSSD

- **LSSD = level-sensitive scan design.**
- **Way to achieve full controllability, observability of registers.**
- **Links all registers in a scan chain.**

LSSD latch



LSSD Advantages/Disadvantages

- **Advantages:**

- 1. The testing problem is transformed from one of sequential circuit testing to one of combinational circuit testing.**
- 2. By adding controllability/observability to the state variables, LSSD also eases functional testing.**

LSSD Advantages/Disadvantages

- **Disadvantages:**

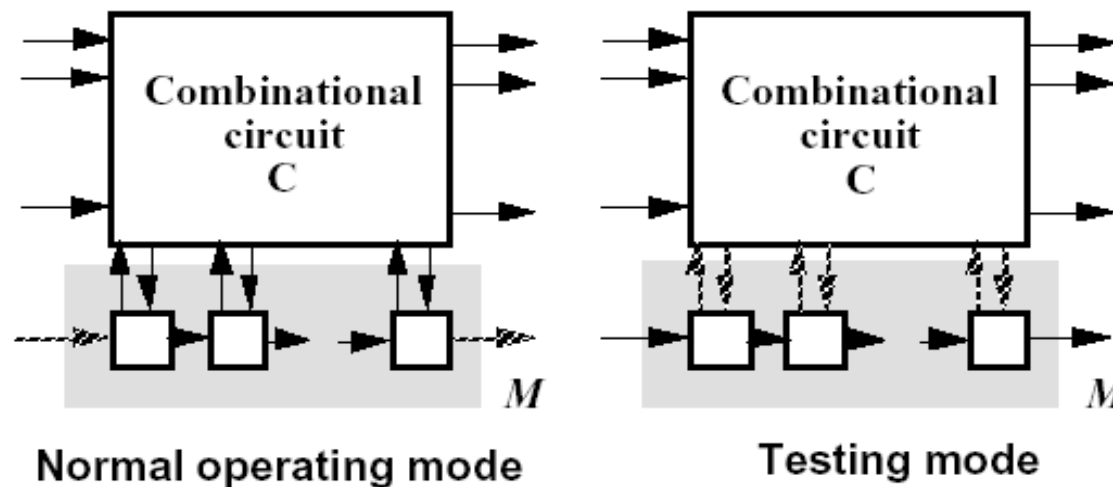
- 1. Additional area for the LSSD latches (area overhead)**
- 2. Additional time required to latch the next state into the LSSD registers (speed overhead)**
- 3. Additional time required to scan in/out test vectors and responses (testing overhead)**
- 4. Clock generation and distribution is more difficult.**

Partial scan

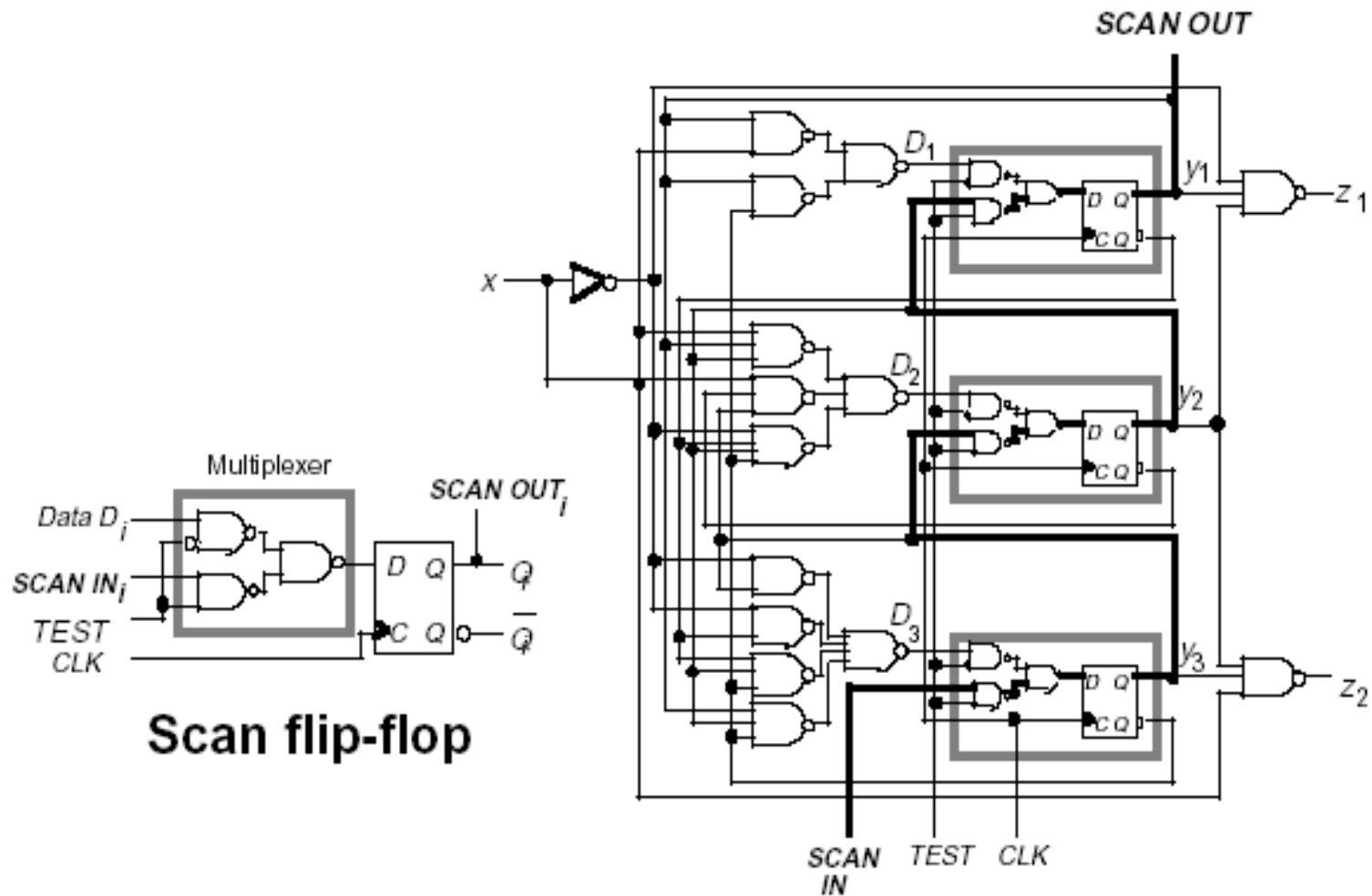
- **Full scan is expensive: must roll out and roll in state many times during a set of tests.**
- **Partial scan selects some registers for scanability.**
- **Requires analysis to choose which registers are best for scan.**

Scan Design

- Flip-flops are reconfigured into a shift register R during testing.
- Test data transferred serially to and from R making the state controllable and observable



Scan path Method



Testing with Scan Design

● Testing Method

1. SCAN IN: Set test mode ($TEST = 1$). Enter initial state into scan register R. Apply test pattern to C.
2. Return to normal mode ($TEST = 0$). Clock circuit through one clock period.
3. SCAN OUT: Set test mode ($TEST = 1$). Read state serially from R. Check state and C's response.

● Features

- Full controllability and observability
- Test patterns needed for C only.
- Hardware overhead is usually small
- Test application is slow