VLSI Design
Lecture 4: Wires and Vias, Parasitics

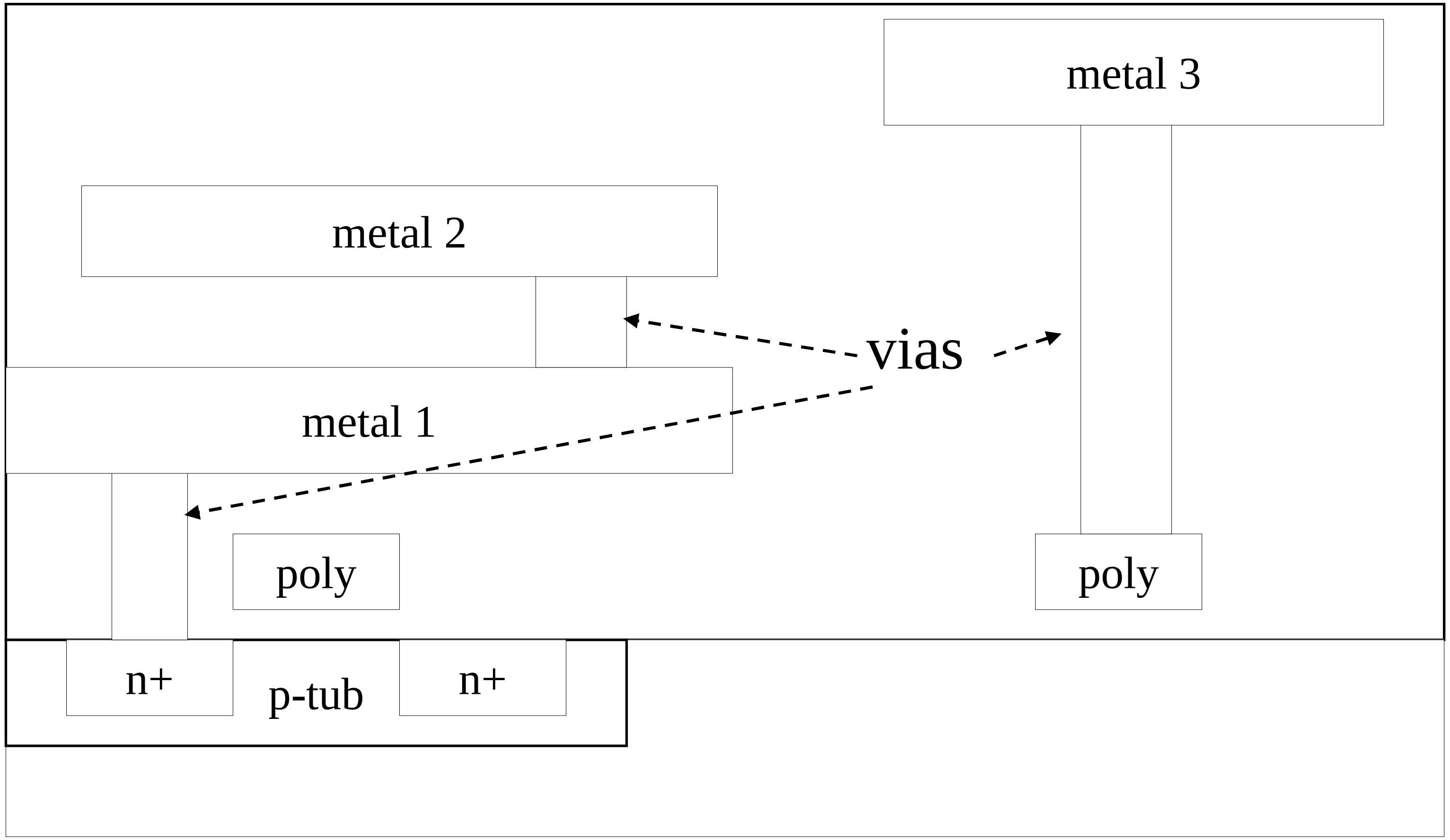
Shaahin Hessabi
Department of Computer Engineering
Sharif University of Technology

Adapted, with modifications, from lecture notes prepared by the author (from Prentice Hall PTR)

Topics

- Wire and via structures
- Wire parasitics
  - Capacitance
  - Resistance
- Transistor parasitics

Wires and vias



Metal migration

- Current-carrying capacity of metal wire depends on cross-section. Height is fixed, so width determines current limit.
- Metal migration: when current is too high, electron flow pushes around metal grains. Higher resistance increases metal migration, leading to destruction of wire.

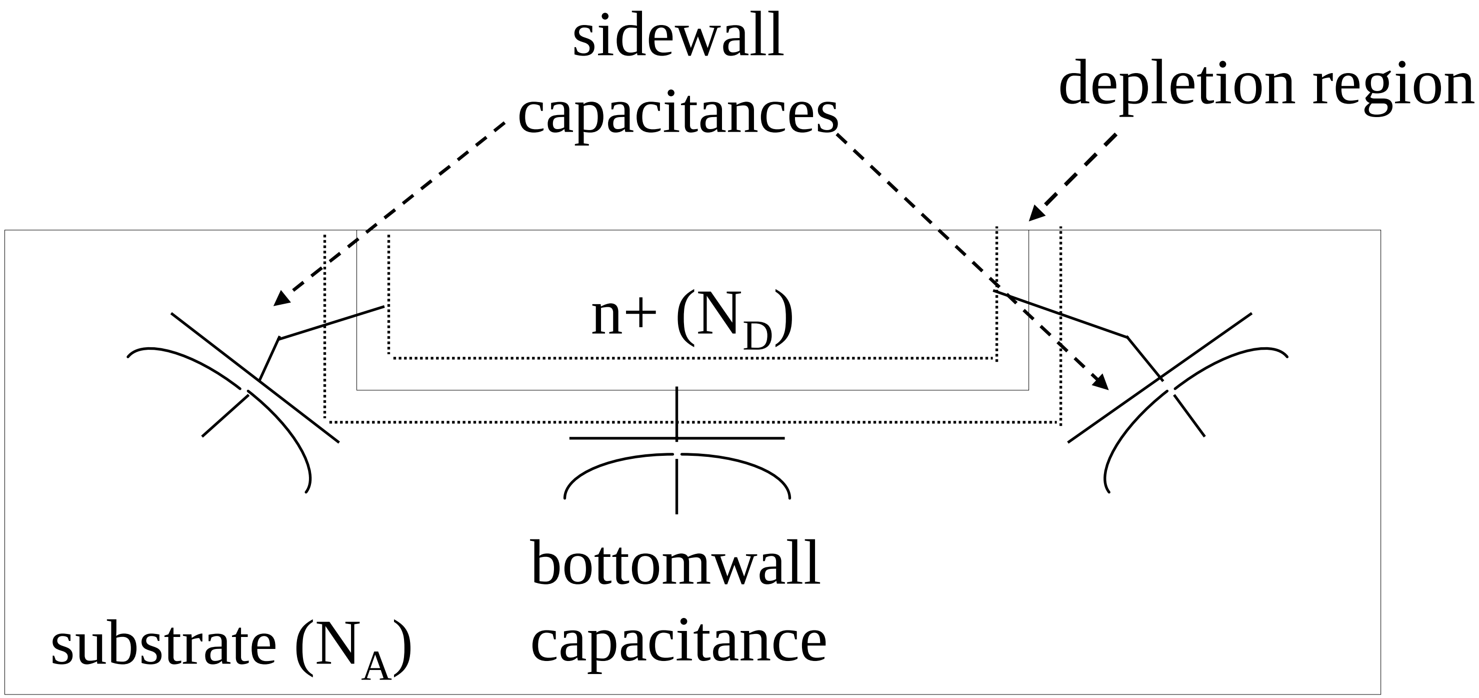
Metal migration problems and solutions

- Marginal wires will fail after a small operating period—*infant mortality*.
- Normal wires must be sized to accommodate maximum current flow:

  I_{max} = 1.5 mA/μm of metal width.
- Mainly applies to V_{DD}/V_{SS} lines.

Diffusion wire capacitance

❖ Capacitances formed by p-n junctions:

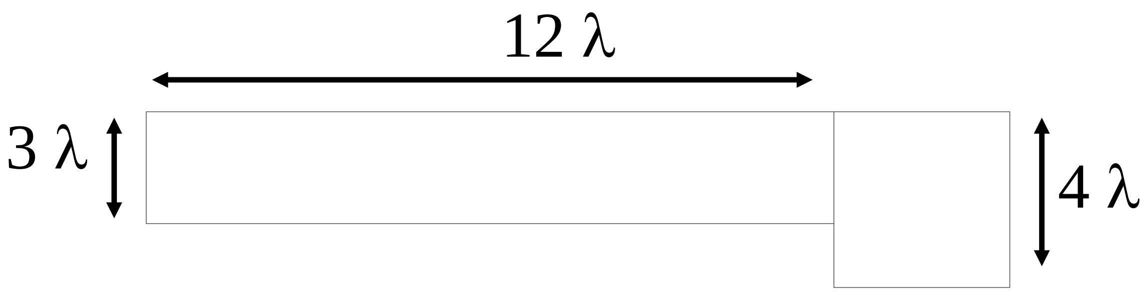


Typical 0.5 micron diffusion capacitance values

- n-type:
  - bottomwall: 0.6 fF/μm^2
  - sidewall: 0.2 fF/μm
- p-type:
  - bottomwall: 0.9 fF/μm^2
  - sidewall: 0.3 fF/μm
- In 0.5 micron process, λ = 0.25 μm

Diffusion capacitance example

- Perimeter = 32λ area = $52\ \lambda^2$
- sidewall/bottomwall capacitances = ?
- total capacitance = ?

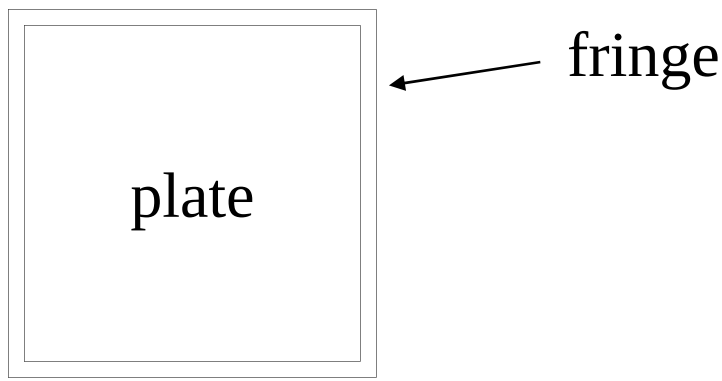


Depletion region capacitance

- Zero-bias depletion capacitance:
  - $C_{j0} = \varepsilon_{si}/x_d$.
- Depletion region width (zero bias):
  - $x_{d0} = sqrt[(1/N_A + 1/N_D)2\varepsilon_{si}V_{bi}/q]$.
- Junction capacitance is function of voltage across junction:
  - $C_j(V_r) = C_{j0}/sqrt(1 + V_r/V_{bi})$

Poly/metal wire capacitance

- Two components:
  - parallel plate;
  - fringe.

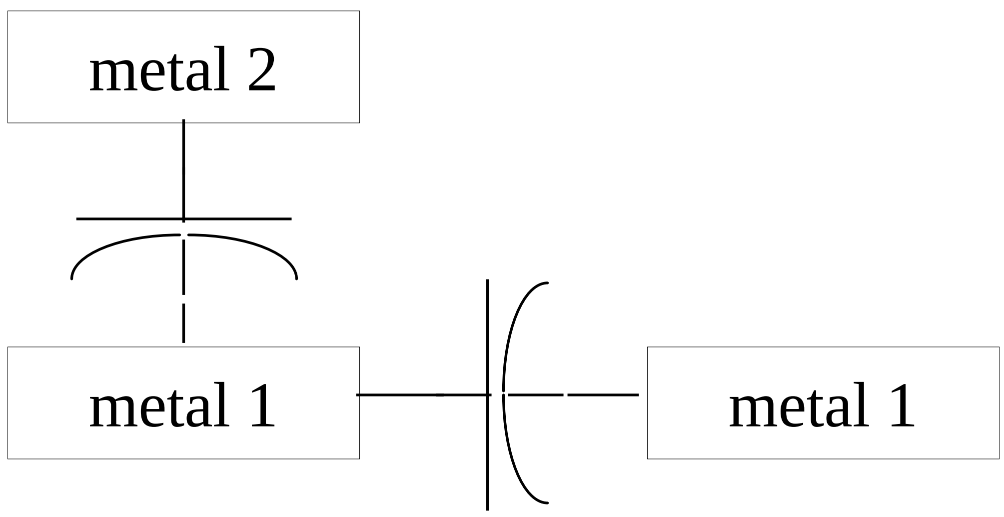


Typical poly/metal capacitance values for 0.5 micron process

- poly:
  - plate: 0.09 $fF/\mu m^2$
  - fringe: 0.04 $fF/\mu m$
- metal 1:
  - plate: 0.04 $fF/\mu m^2$
  - fringe: 0.09 $fF/\mu m$
- metal 2:
  - plate: 0.02 $fF/\mu m^2$
  - fringe: 0.06 $fF/\mu m$
- metal 3:
  - plate: 0.009 $fF/\mu m^2$
  - fringe: 0.02 $fF/\mu m$

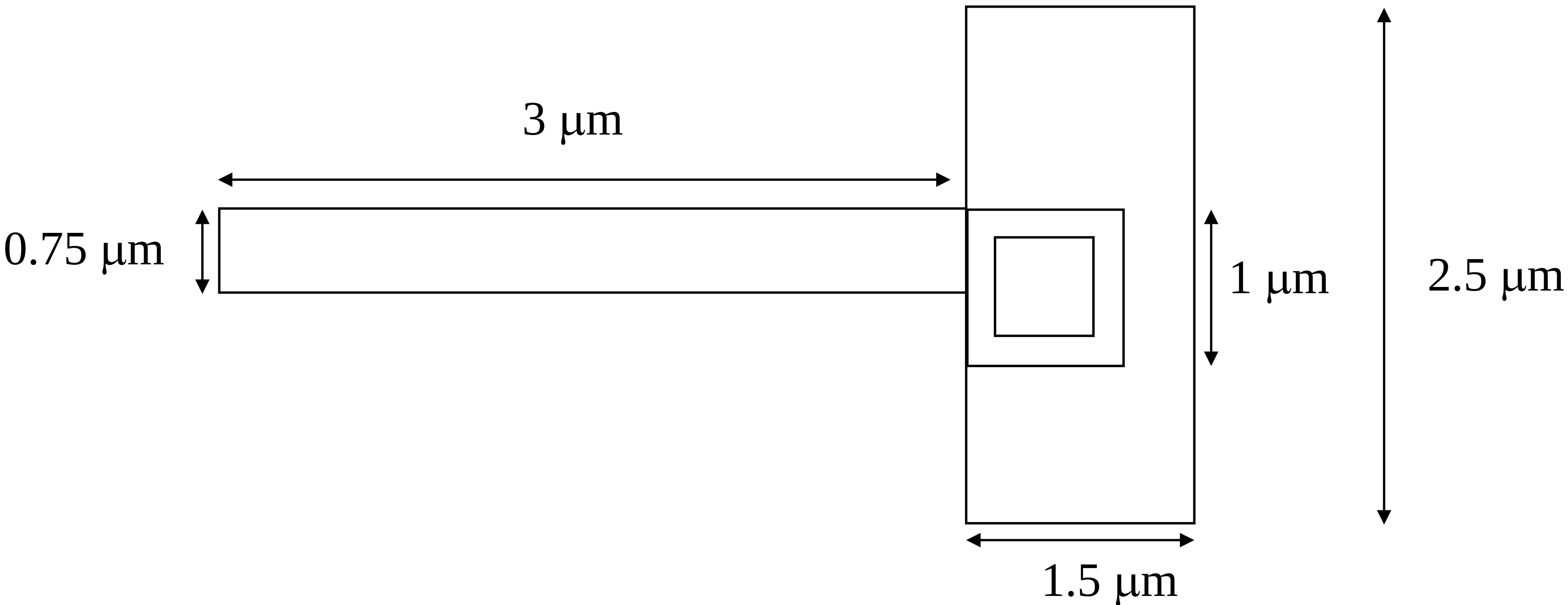
Metal coupling capacitances

- Can couple to adjacent wires on same layer, and to wires on above/below layers:



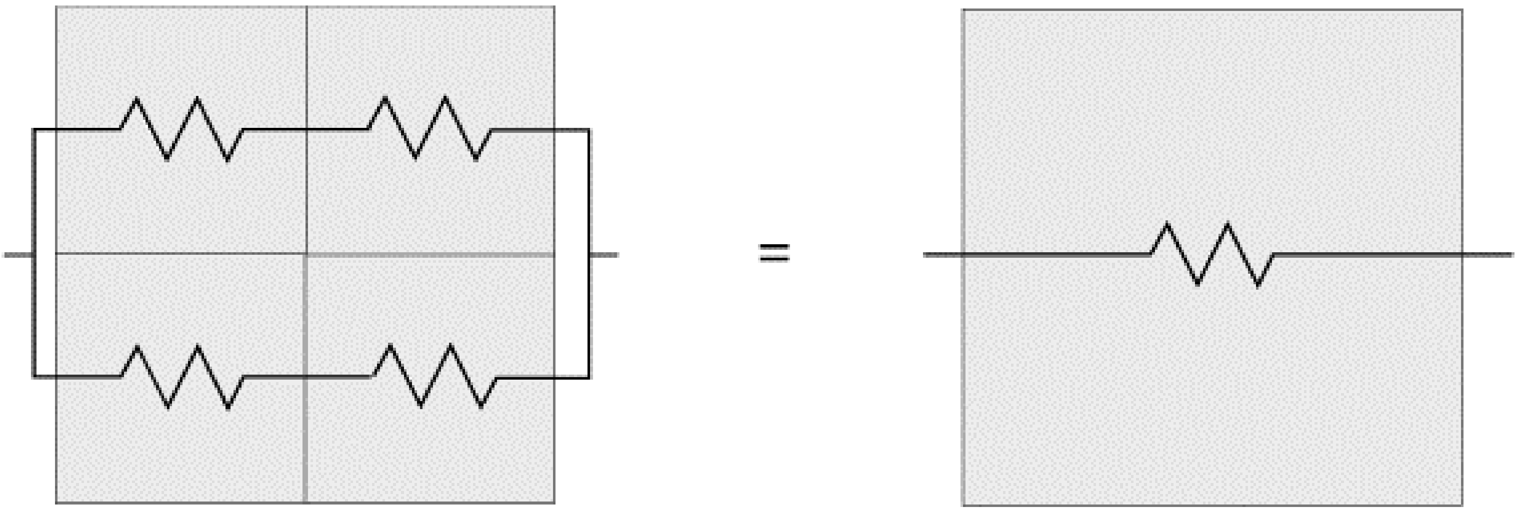
Example: parasitic capacitance measurement

- n-diffusion: bottomwall=2 fF,
  sidewall=2 fF.
- metal: plate=0.15 fF, fringe=0.72 fF.



Wire resistance

- ❖ Resistance of any size square is constant:

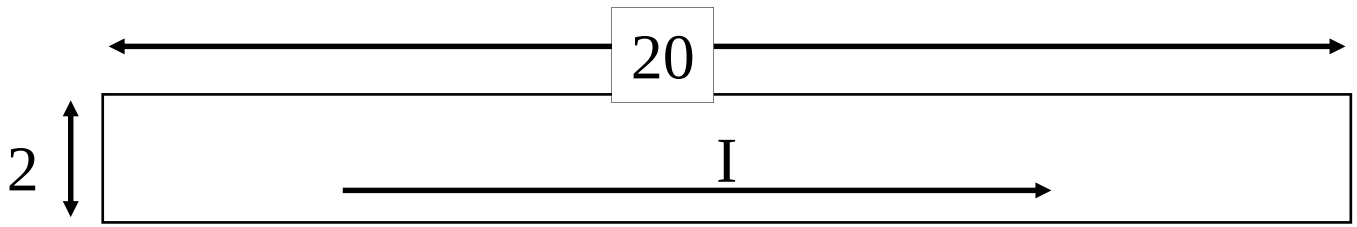


Typical resistance values for our 0.5 micron process

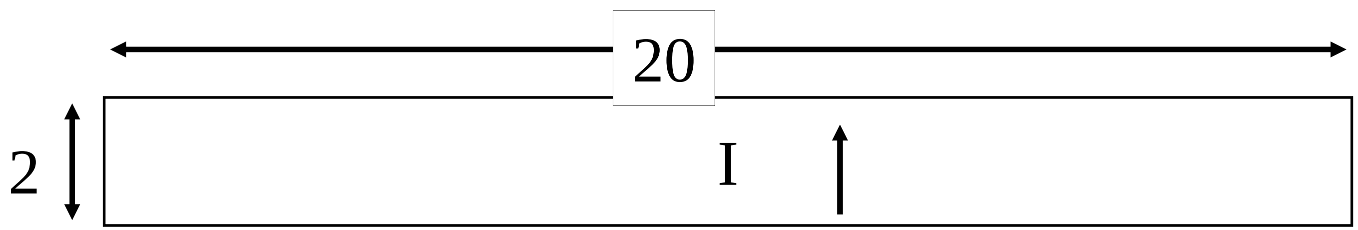
- Poly: 4 ohms/square
- metal 1: 0.08 ohms/square
- metal 2: 0.07 ohms/square
- metal 3: 0.03 ohms/square
- ndiff: 2 ohms/square
- pdiff: 2 ohms/square

Calculating resistance

❖ Determine current flow, then aspect ratio:

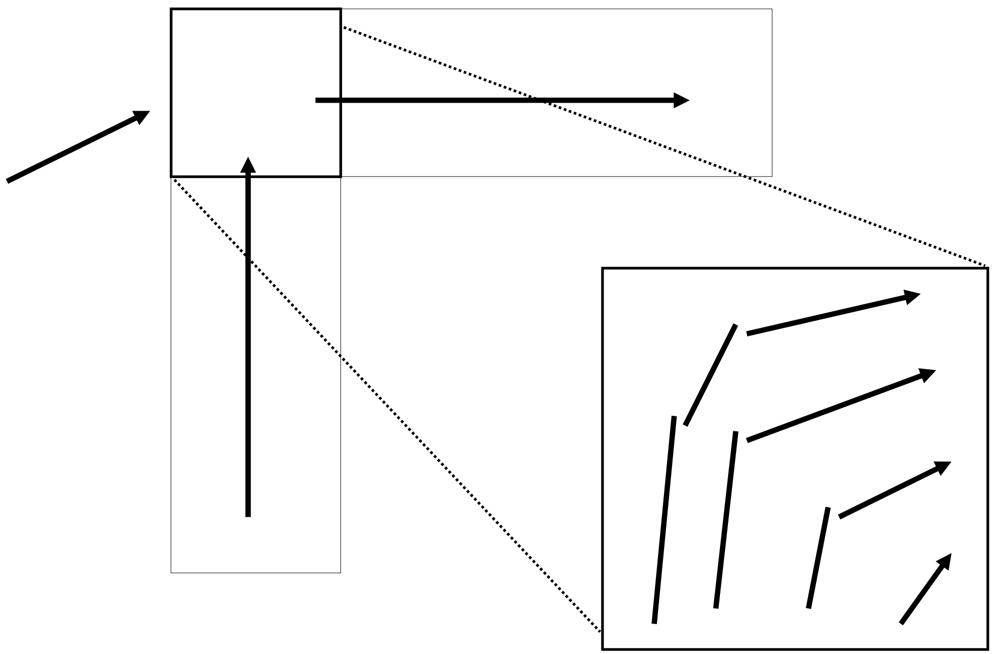


vs.



Current around corners

- Resistance at corner of two equal-width wires is approximately 1/2 square:



Via resistance

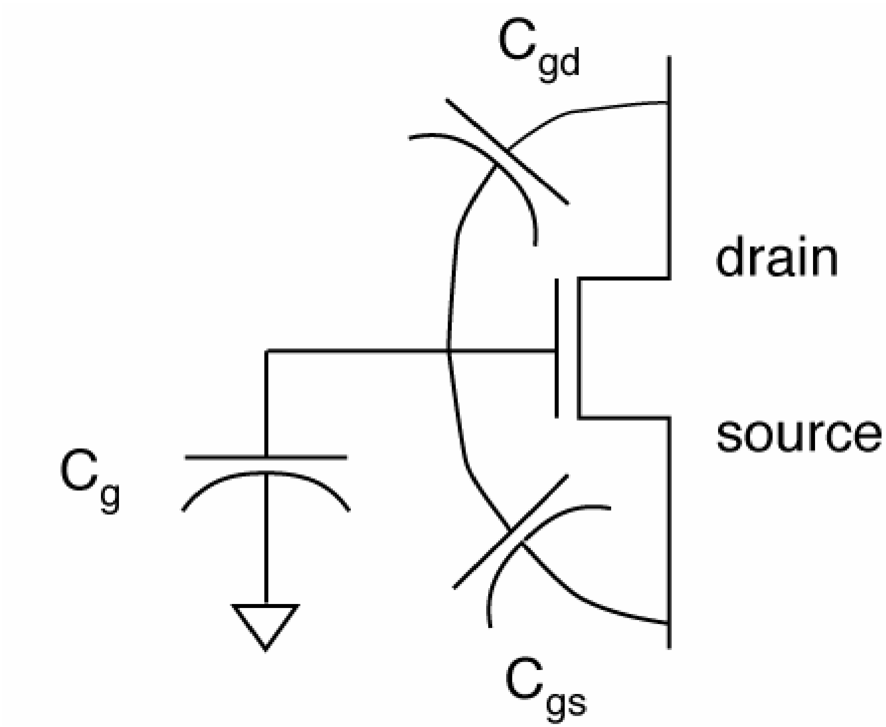
- Determined by current flow through via cut.
- Typical metal1-poly contact: 2.5 ohms.
- Typical metal1-metal2 contact: 0.5 ohms.

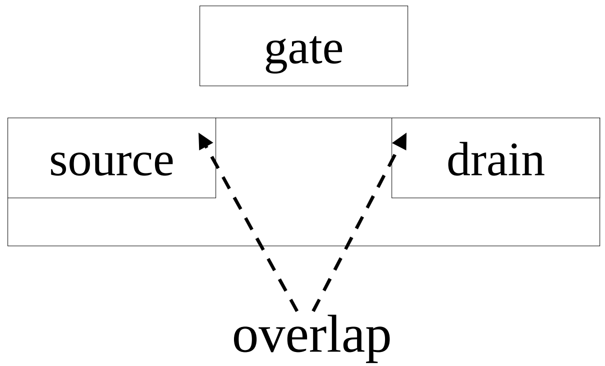
Skin effect

- At low frequencies, most of copper conductor's cross section carries current.
- As frequency increases, current moves to skin of conductor.
  - Back EMF induces counter-current in body of conductor.
- Skin effect most important at gigahertz frequencies.

Transistor gate parasitics

- ❖ Gate-source/drain overlap capacitance:





Transistor source/drain parasitics

- Source/drain have significant capacitance, resistance.
  - Significant effect on circuit performance.
- Measured same way as for wires.
- Source/drain R, C may be included in Spice model rather than as separate parasitics.