

# **VLSI Design**

## **Lecture 2: Basic Fabrication Steps and Layout**

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Adapted with modifications from lecture notes  
prepared by author (from Prentice Hall PTR)

# Topics

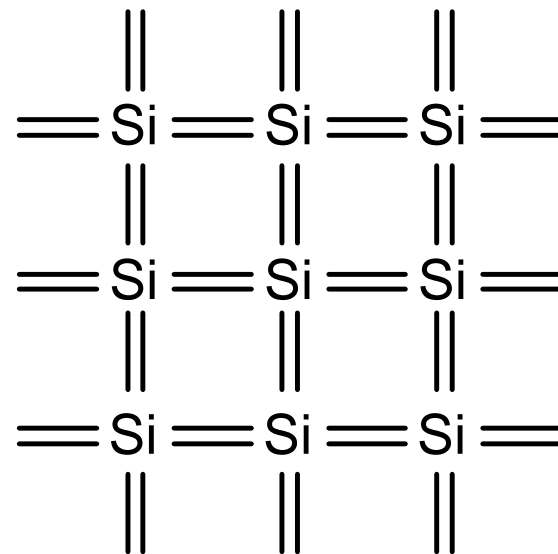
- Basic fabrication steps.
- Transistor structures.
- Basic transistor behavior.
- Latch up.

# Fabrication services

- Educational services:
  - U.S.: MOSIS
  - EC: EuroPractice
  - Taiwan: CIC
  - Japan: VDEC
- Foundry = fabrication line for hire.
  - Foundries are major source of fab capacity today.

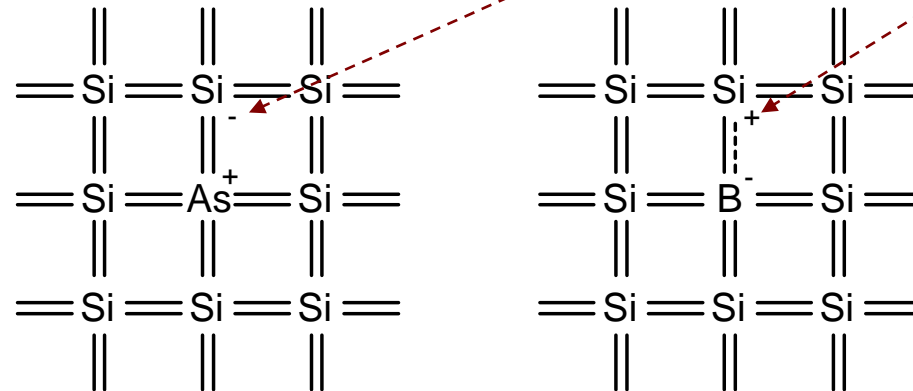
# Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



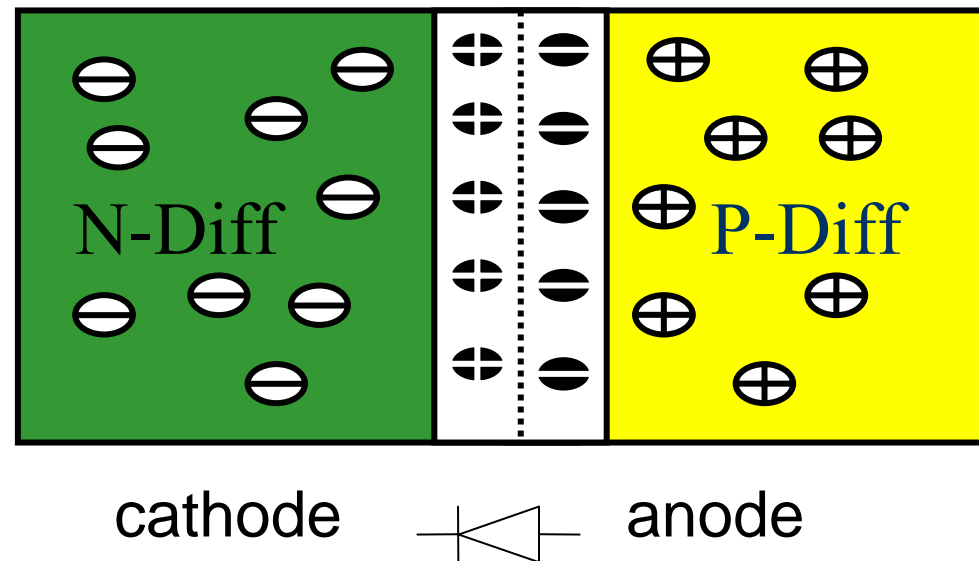
# Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V (Arsenic, Phosphorus): extra electron (n-type)
- Group III (Boron): missing electron, called hole (p-type)



# *p-n Junctions*

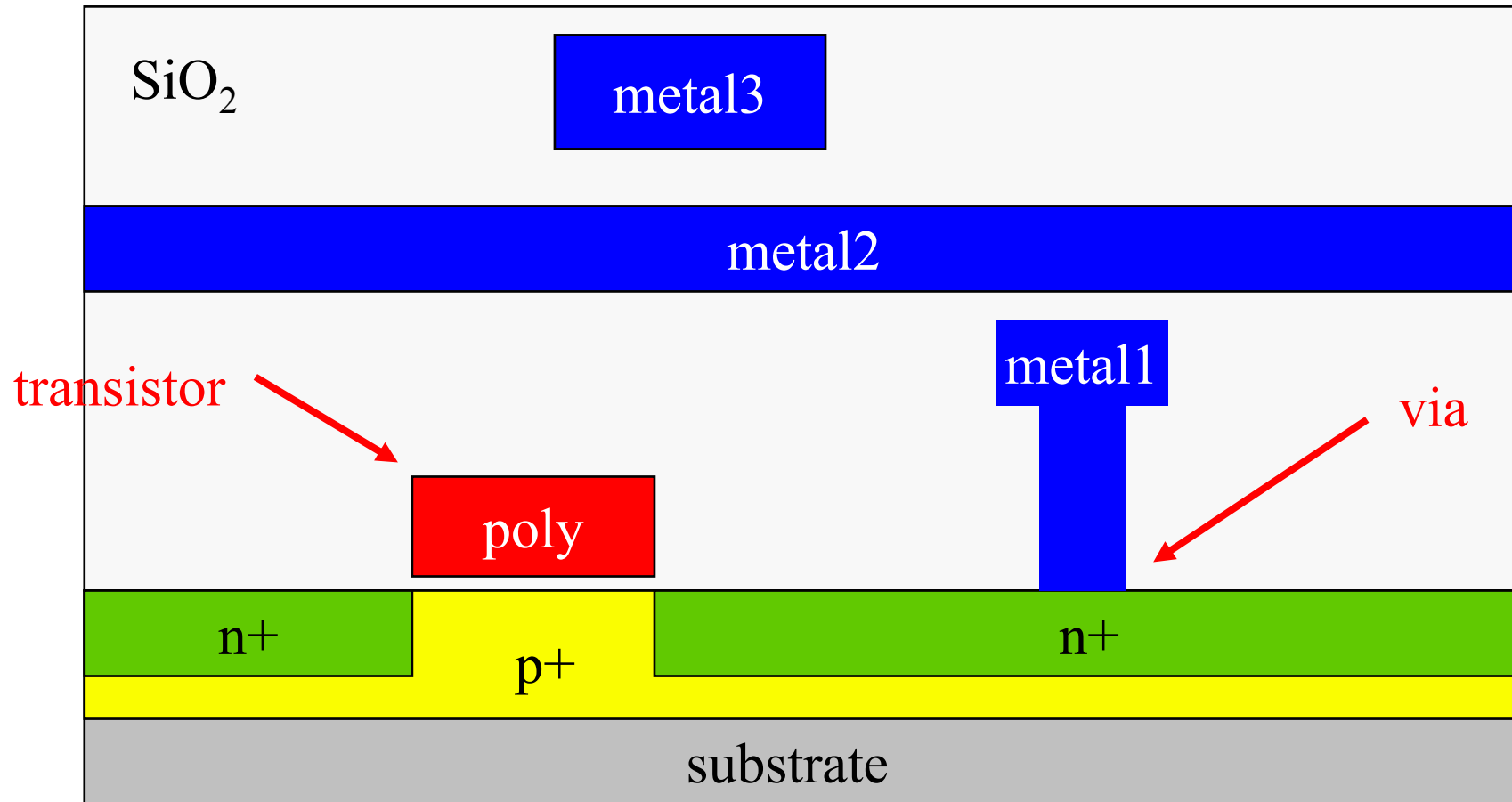
- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



# Fabrication processes

- IC built on silicon substrate:
  - some structures diffused into substrate;
  - other structures built on top of substrate.
- Substrate regions are doped with n-type and p-type impurities. (n+ = heavily doped)
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum (metal).
- Silicon dioxide (SiO<sub>2</sub>) is insulator.

# Simple cross section



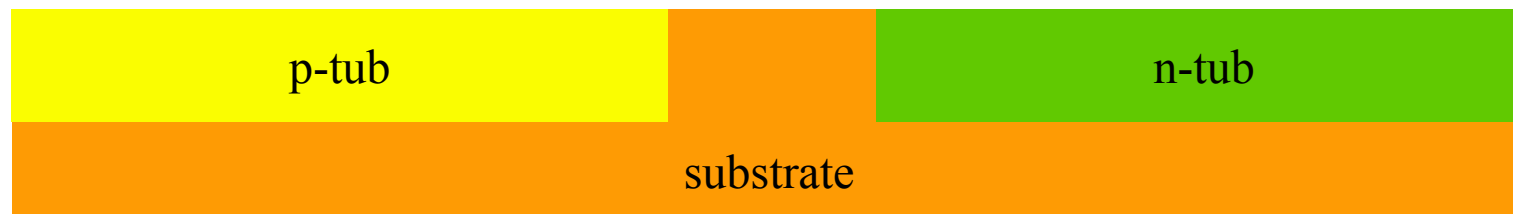
# Photolithography

Mask patterns are put on wafer using photo-sensitive material:

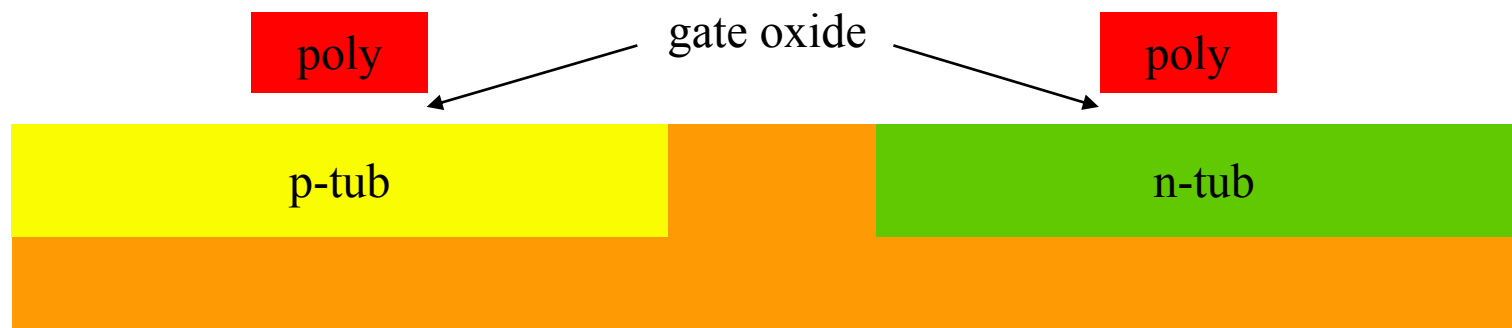


# Process steps

First place tubs to provide properly-doped substrate for n-type, p-type transistors:

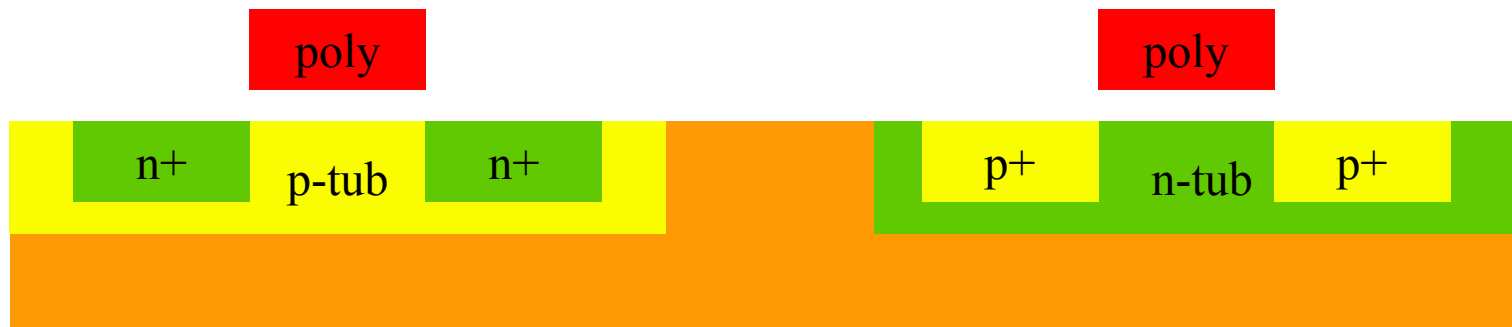


Pattern polysilicon before diffusion regions:



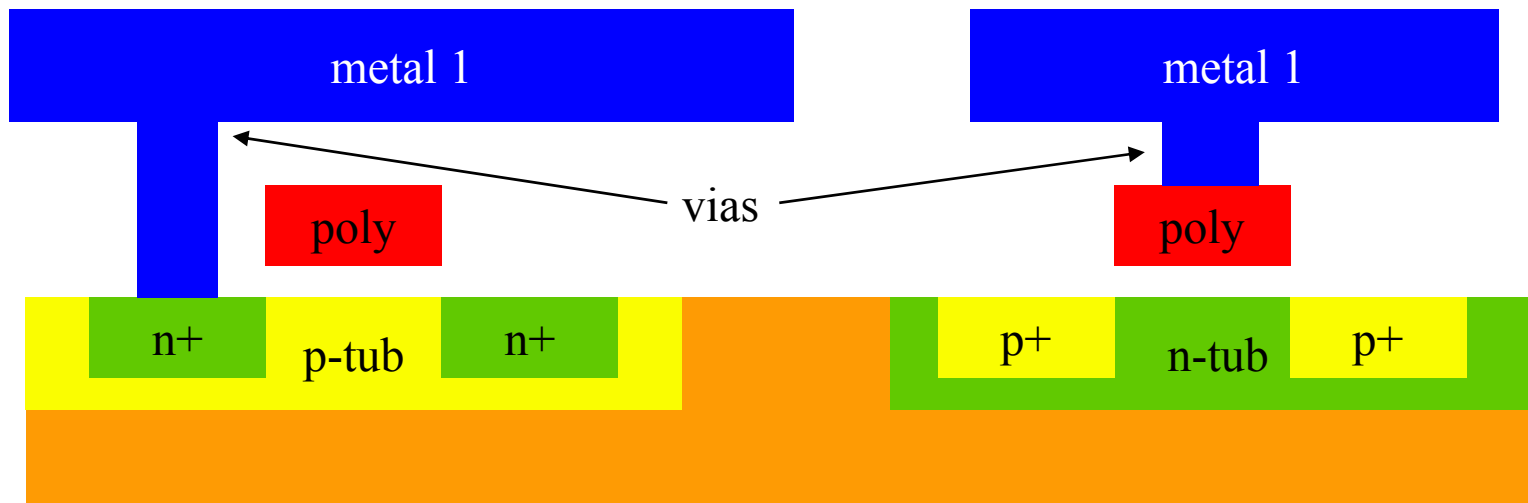
# Process steps, cont'd

Add diffusions, performing self-masking:



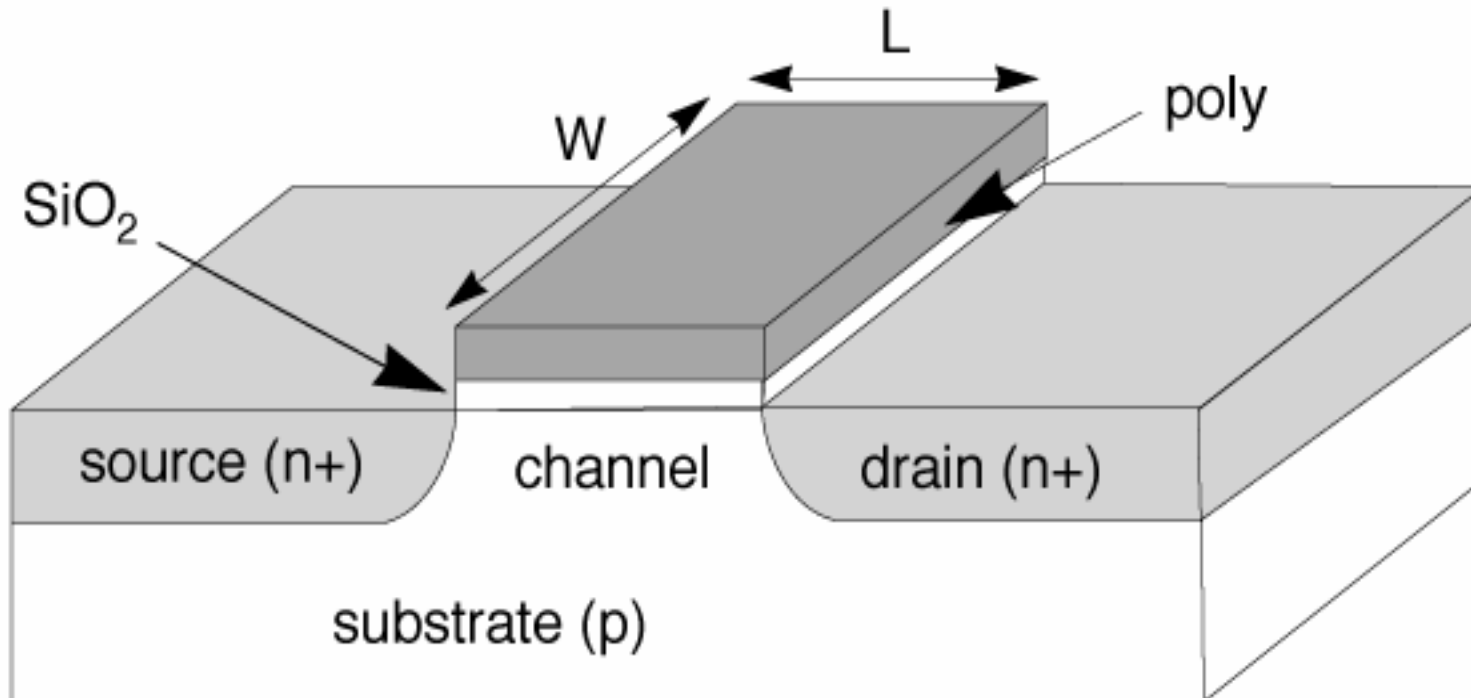
# Process steps, cont'd

Start adding metal layers:

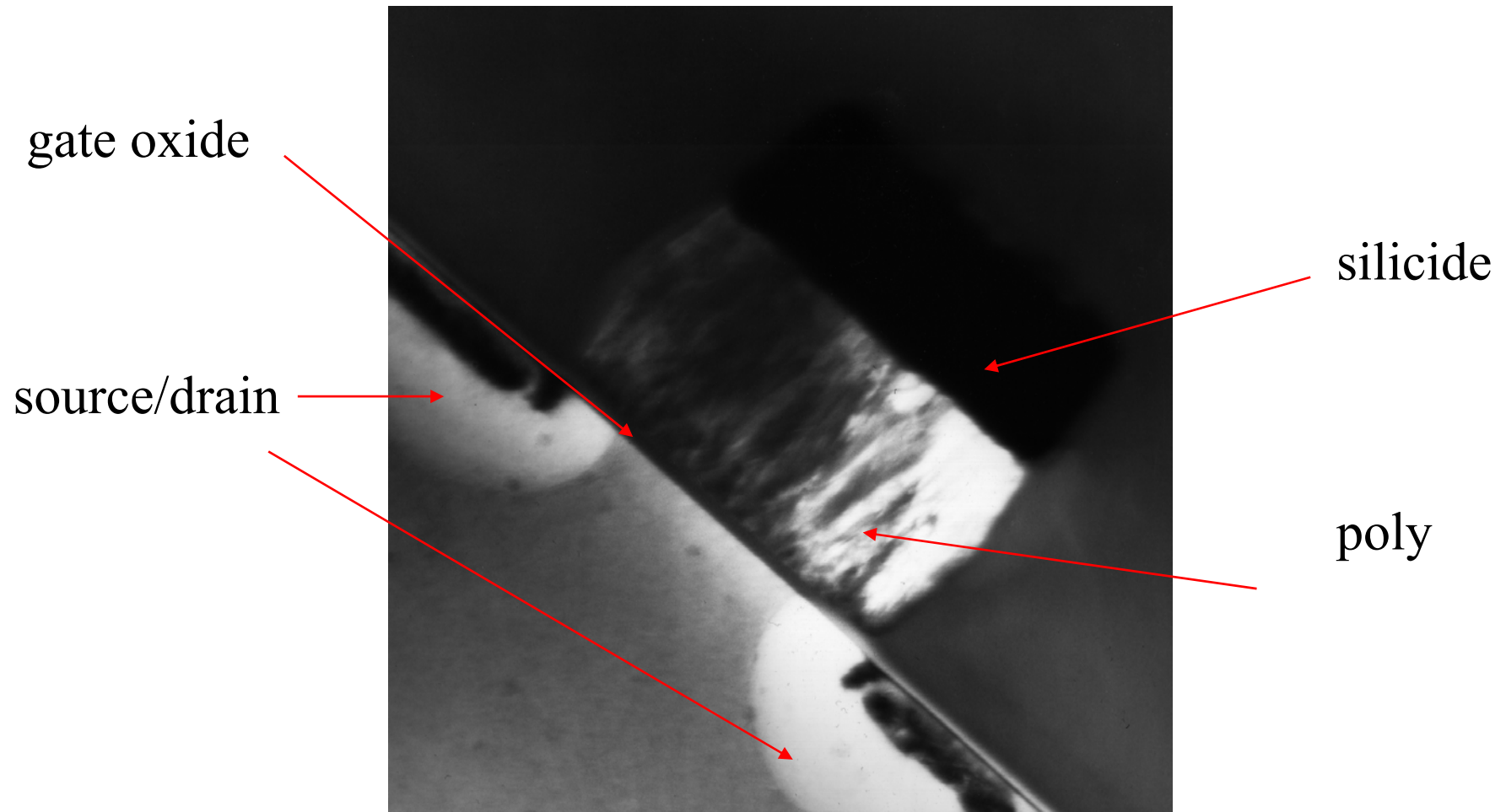


# Transistor structure

n-type transistor:

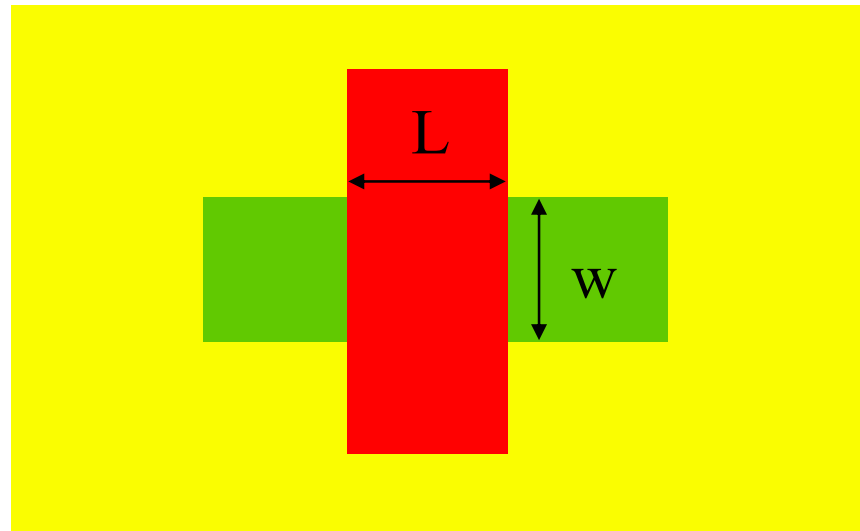


# 0.25 micron transistor (Bell Labs)



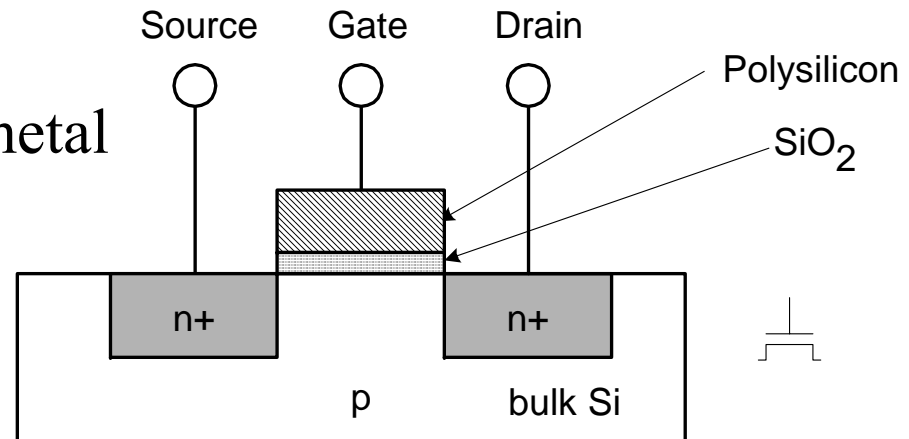
# Transistor layout

n-type (tubs may vary):



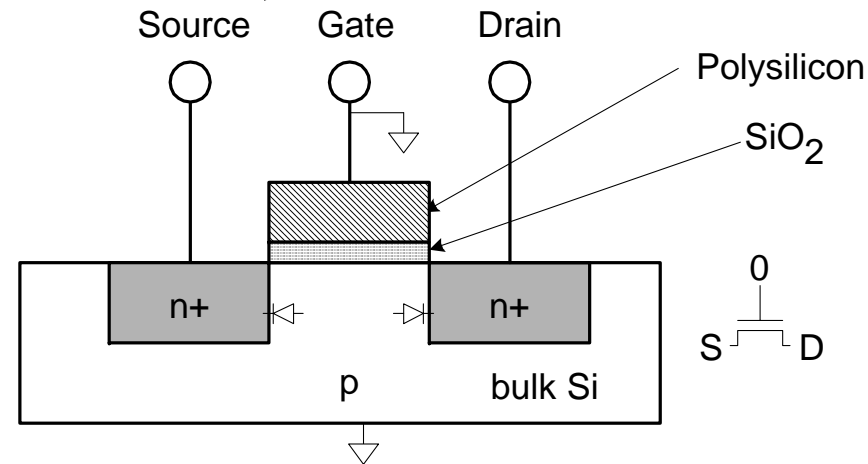
# NMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - $\text{SiO}_2$  (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
    - » Even though gate is no longer made of metal



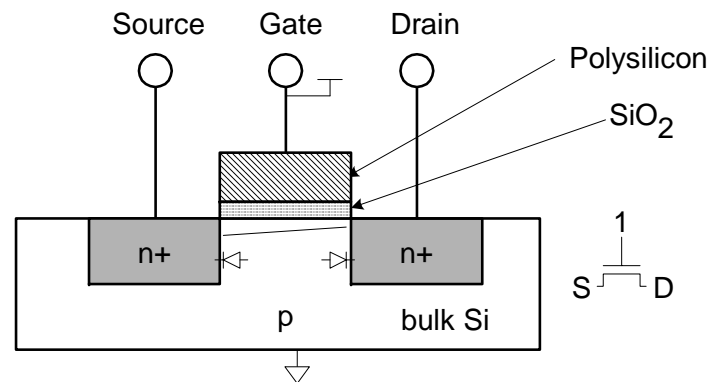
# NMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P type body is at low voltage
  - Source body and drain body diodes are OFF
  - No current flows, transistor is OFF



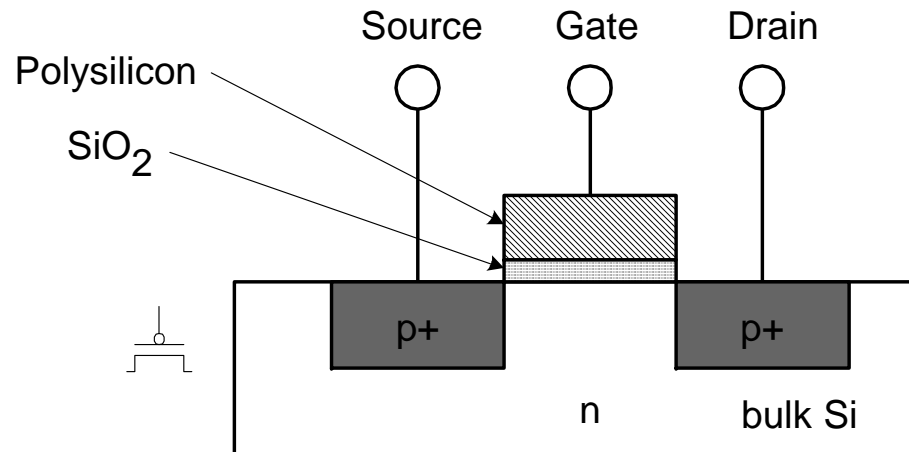
# NMOS Operation (cont'd.)

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n type
  - Now current can flow through n type silicon from source through channel to drain, transistor is ON

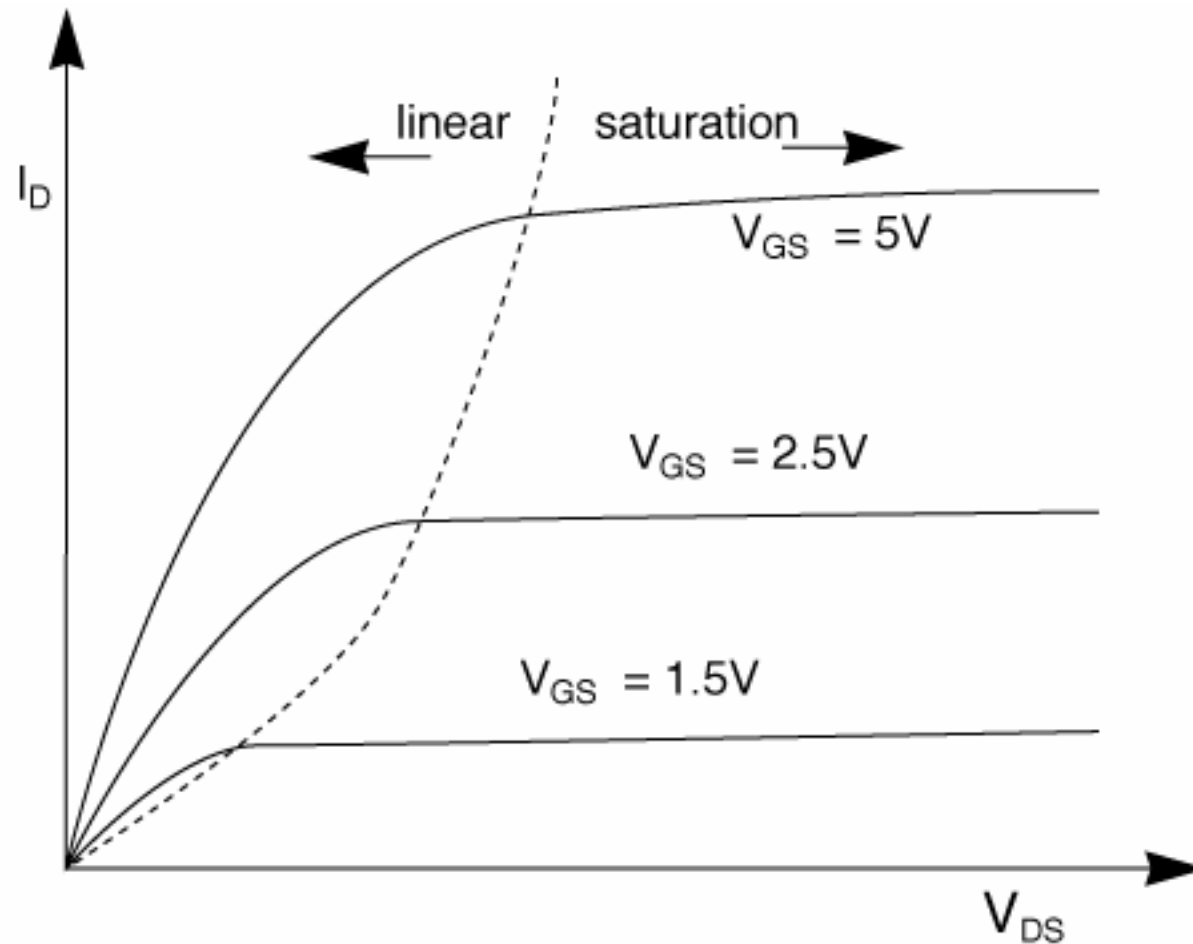


# PMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage ( $V_{DD}$ )
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



# Drain current characteristics



# Drain current

- Linear region ( $V_{ds} < V_{gs} - V_t$ ):
  - $I_d = k' (W/L)[(V_{gs} - V_t)V_{ds} - 0.5 V_{ds}^2]$
- Saturation region ( $V_{ds} \geq V_{gs} - V_t$ ):
  - $I_d = 0.5k' (W/L)(V_{gs} - V_t)^2$

# 0.5 $\mu\text{m}$ transconductances

From a MOSIS process:

- n-type:

- $k_n' = 73 \mu\text{A}/\text{V}^2$

- $V_{tn} = 0.7 \text{ V}$

- p-type:

- $k_p' = 21 \mu\text{A}/\text{V}^2$

- $V_{tp} = -0.8 \text{ V}$

# Current through a transistor

Use 0.5  $\mu\text{m}$  parameters. Let  $W/L = 3/2$ . Measure at boundary between linear and saturation regions:

- $V_{gs} = 2V$ :

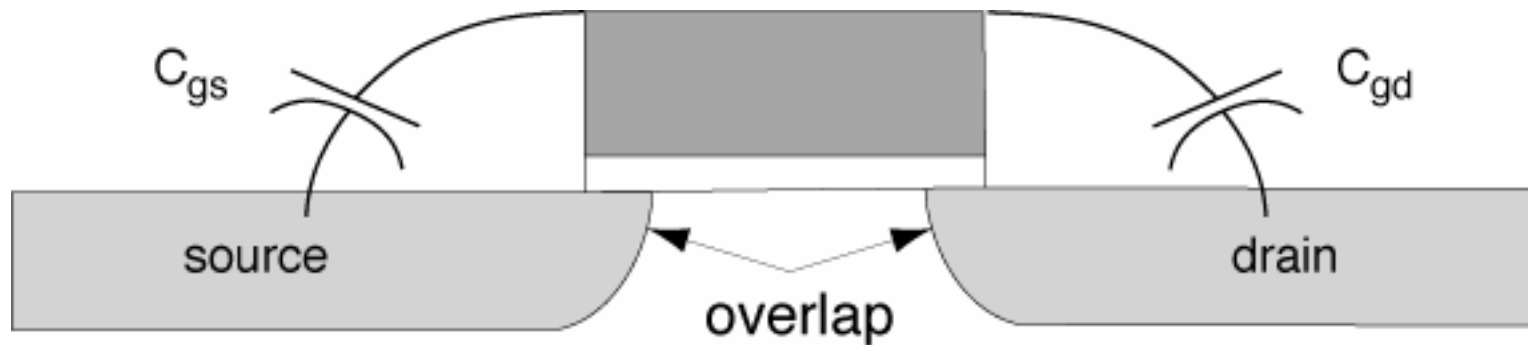
$$I_d = 0.5k'(W/L)(V_{gs} - V_t)^2 = 93 \mu\text{A}$$

- $V_{gs} = 5V$ :

$$I_d = 1 \text{ mA}$$

# Basic transistor parasitics

- Gate to substrate, also gate to source/drain.
- Source/drain capacitance, resistance.



# Basic transistor parasitics, cont'd

- Gate capacitance  $C_g$ . Determined by active area.
- Source/drain overlap capacitances  $C_{gs}$ ,  $C_{gd}$ .  
Determined by source/gate and drain/gate overlaps.  
Independent of transistor  $L$ .
  - $C_{gs} = C_{ol} W$
- Gate/bulk overlap capacitance.

# Latch-up

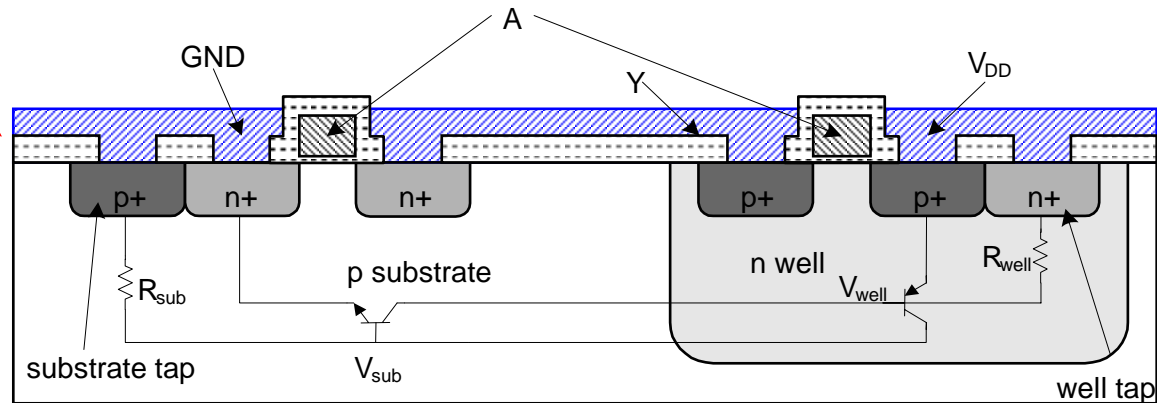
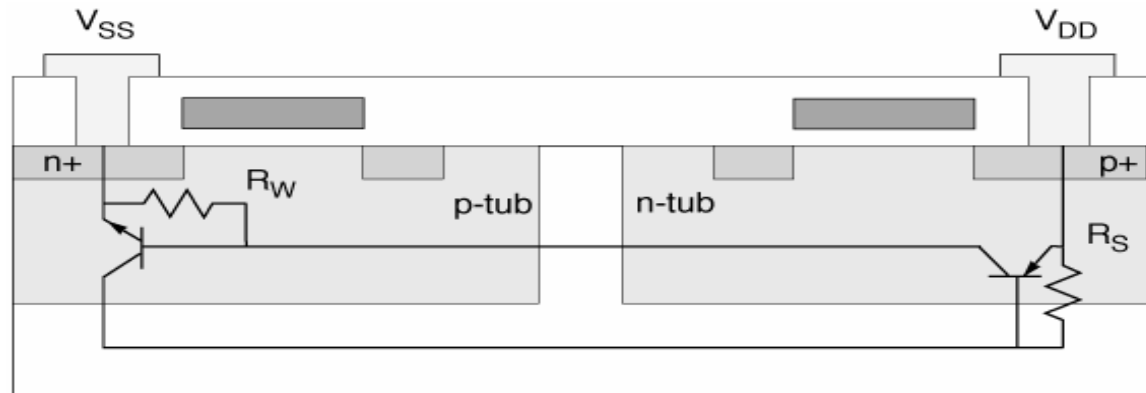
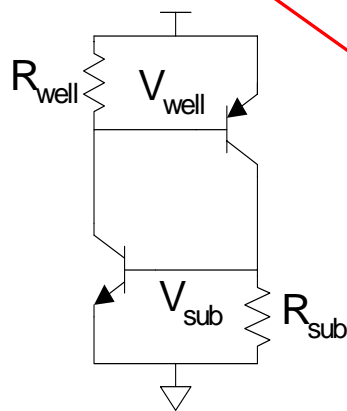
- CMOS ICs have parasitic silicon-controlled rectifiers (SCRs).
- When powered up, SCRs can turn on, creating low-resistance path from power to ground. Current can destroy chip.
- Early CMOS problem. Can be solved with proper circuit/layout structures.

# Parasitic SCR structure

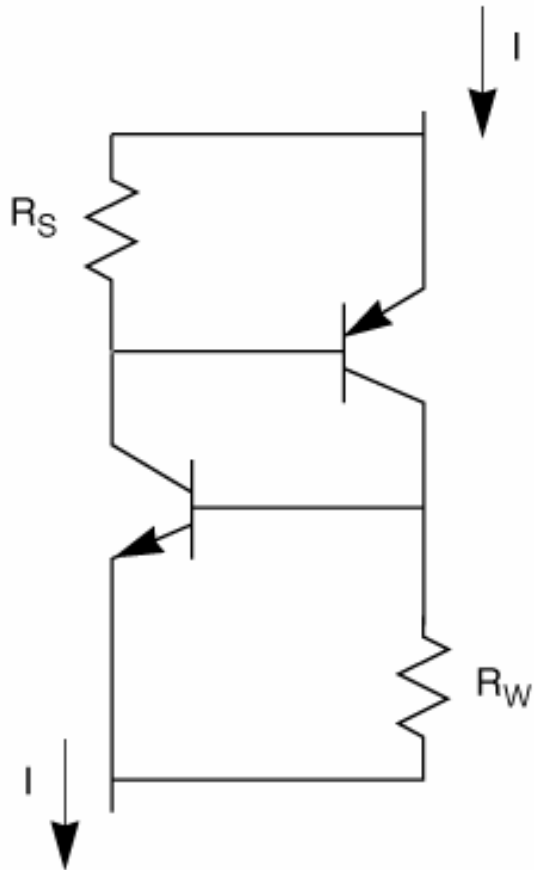
- There exist parasitic bipolar transistors (pnp and npn) in a CMOS structure.
- Additionally, the well and substrate have resistances  $R_W$  and  $R_S$ , respectively.

Twin tub

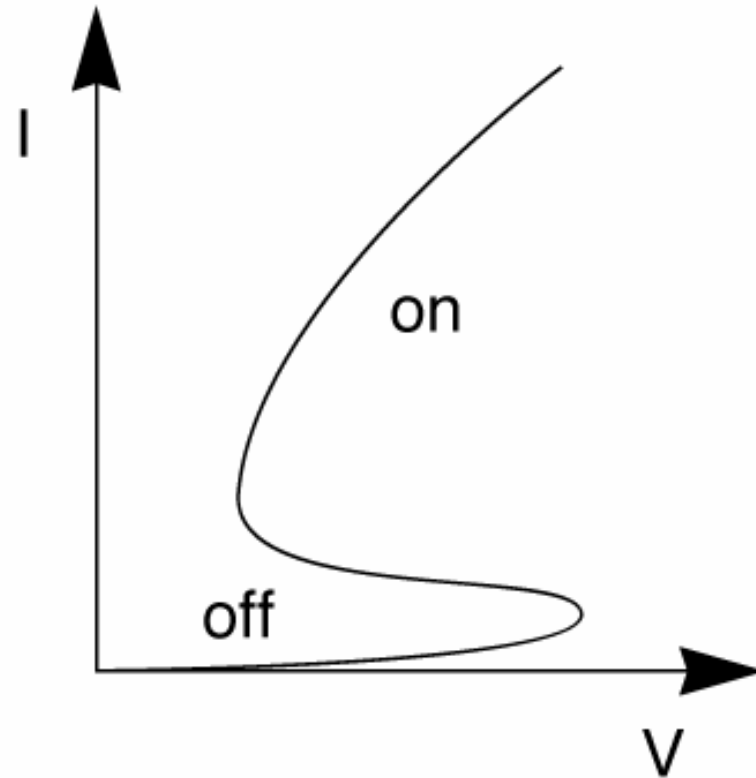
n tub



# Parasitic SCR



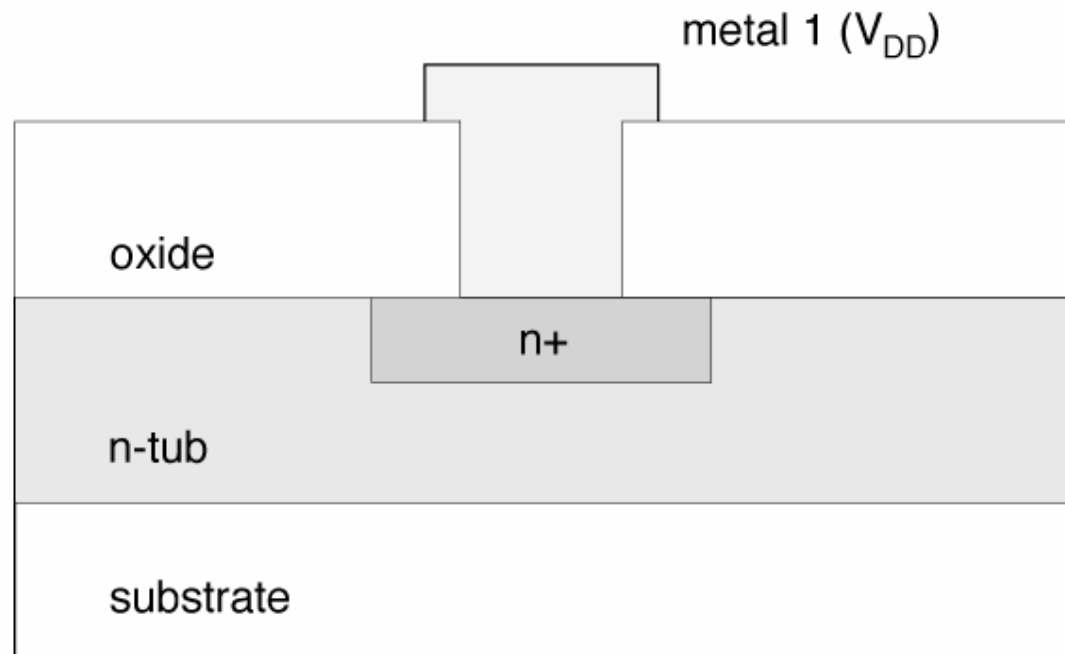
circuit



$I$   $V$  behavior

# Solution to latch-up

Use tub ties to connect tub to power rail. Use enough to create low-voltage connection.



# Tub tie layout

