# Millimeter-Wave Reflective-Type Phase Shifter in CMOS Technology

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***Abstract*—The design and measurement of a compact, wide-band reflective-type phase shifter in 90 nm CMOS technology in V-band frequency is presented. This phase shifter has a fractional bandwidth of 26% and an average insertion loss of 6 dB over all phase states. The chip area is only 0.08 mm$^2$. Measurement results show that the developed phase shifter provides 90° continuous phase shift over the frequency range of 50–65 GHz. The measured return loss is greater than 12 dB at 50 GHz. The output power is linear up to at least 4 dBm input power.**

***Index Terms*—CMOS, millimeter wave, reflective type phase shifter, 60 GHz.**

## I. Introduction

PHASED array technology is the ultimate solution for Non-Line-of-Sight (NLOS) millimeter-wave (mm-wave) communication. The fast growing short-range wireless applications, such as Wireless Personal Area Network (WPAN), require wideband devices operating from 57 to 64 GHz in North America. Furthermore, the success of silicon integration over the last decade has motivated the research and investment on low-power integrated mm-wave phased arrays in silicon [1].

The phase shifter is the key component of a phased array system. A substantial body of research has been conducted on developing different types of phase shifters [2]–[6]. A compact, low-power and linear phase shifter lowers the cost and complexity of the phased array system, significantly. Although designing such a phase shifter is a challenge, the variation of the overall loss of the phase shifter versus the control voltage (or number of bits) is the crucial problem, which can deteriorate the phased array gain to a large extent [7]. Active phase shifters reduce loss variations. Indeed, interesting results in terms of chip area, linearity and insertion loss have been achieved at K-band [2] and Q-band [3]. Nevertheless, at V-band the reported works suffer from high insertion loss [5] or power consumption [6].

An analog phase shifter provides a continuous phase shift, which reduces the beam-pointing error of the phased array antenna. Furthermore, it has been shown that a continuous phase shifter results in the lowest error vector magnitude (EVM) compared to 3, 4, and 5-bit digital phase shifters [8].

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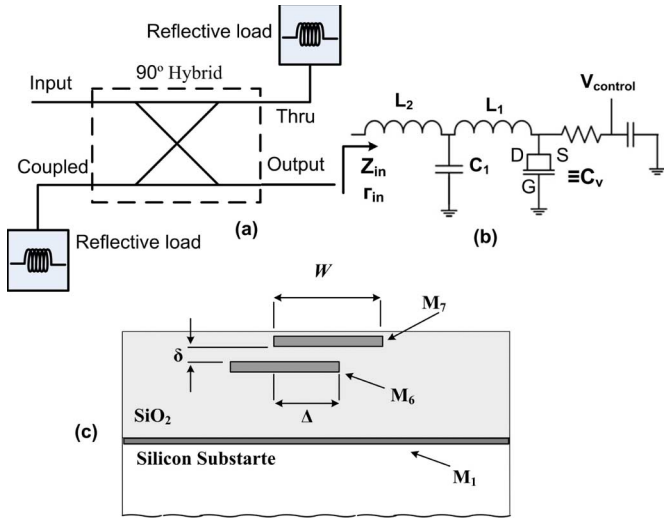


Fig. 1. (a) General block diagram of the reflective-type phase shifter. (b) The proposed reflective load. (c) Cross section of the broadside structure implemented in CMOS technology.

In this letter, a broadband Reflective-Type Phase Shifter (RTPS) at V-band is designed in 90 nm CMOS technology. This RTPS provides 90 degree continuous phase shift over the frequency band of 50–65 GHz. The mean insertion loss of the phase shifter is 6 dB for all phase states. This device needs only one control voltage to adjust the phase shift. Compared to active phase shifters, this passive device has negligible dc power consumption and a small chip area (0.08 mm$^2$). To the best of the authors' knowledge, this is the *first* reported RTPS in CMOS technology at V-band.

In the following, the design steps of the proposed phase shifter as well as the measurement results will be explained.

## II. Reflective-Type Phase Shifter in CMOS Technology

Fig. 1(a) shows the general block diagram of the RTPS. The reflected signals from the reflective loads are added in-phase at the output port, while the out of phase signals at the input port provide good matching conditions for the phase shifter. The maximum phase shift depends on the load type.

### A. Reflective Load Design

In the integrated RTPS design, varactors are used in the design of the reflective loads. Varactors can be implemented in CMOS technology by using a regular CMOS transistor in which the source and drain terminals are connected together. Applying a variable voltage between the gate and drain/source of this structure generates a variable capacitor. Assume a transistor

with $W = 7\ \mu$m and $L = 0.37\ \mu$m, where $W$ and $L$ are width and length of the transistor, respectively. The high-frequency device simulation demonstrates that, at 60 GHz frequency, by varying the applied dc voltage from 0 to 1 V, the transistor functions as a varactor with a minimum capacitance $(\mathrm{C_{v,min}})$ of 49 fF and a tuning ratio of 3. The proposed reflective load is shown in Fig. 1(b). This load contains two inductors, a capacitor and a varactor. The input impedance of this load, for ideal inductors and capacitors is given by

$$Z_{\mathrm{in}} = j\left(\frac{\omega^2 L_1 C_v - 1}{\omega C_v + \omega C_1 - \omega^3 C_v C_1 L_1} + \omega L_2\right) \qquad (1)$$

where $C_v$ denotes the varactor capacitance and $C_1, L_1$ and $L_2$ are the capacitance and inductance of the matching elements shown in Fig. 1(b). The phase of the reflection coefficient can be expressed as

$$\theta = -2\tan^{-1}\left(\frac{\mathrm{Im}(Z_{\mathrm{in}})}{Z_0}\right). \qquad (2)$$

The output phase of the phase shifter changes with $\theta$, which itself depends on varactor capacitance, $C_v$. By setting $L_1 = (\omega^2 C_{v,\min})^{-1}, C_1 = C_{v,\max}/(\omega^2 L_1 C_{v,\max} - 1)$ and $L_2 = 0$, the output phase changes from 0° to 180°. In practice, the resistive parts of the inductors and capacitors limit the overall phase shift of the phase shifter and add to the insertion loss. By optimizing $L_1, L_2$ and $C_2$, (at 170 pH, 60 pH and 60 fF, respectively) an optimum load with minimum loss and more than 90° phase shift over the frequency range of interest is attained.

### *B. 90° Hybrid Design*

For a broadband 90° hybrid, a broadside coupler is utilized. This structure has a broadband behavior. Moreover, it is shielded from the lossy silicon substrate, which is the main source of loss for passive devices on CMOS. As shown in Fig. 1(c), a broadside coupler consists of two parallel microstrip lines on different layers in a multi-layer transmission line structure. The propagating mode of a symmetric broadside coupler can be decomposed into the even and odd modes. Each mode has its specific characteristic impedance. The closed form expressions for the even and odd characteristic impedances of the symmetric broadside coupler can be used for the initial design [9]. The broadside structure is implemented using the thick metals of the CMOS process. The two coupled lines are designed at the metal layers 6 and 7 of the 90 nm CMOS process, where the distance between the metal layers is 0.75 $\mu$m. The physical parameters of the broadside coupler, i.e., line width and position of the coupled lines, shown by $W$ and $\Delta$ in Fig. 1(c), are optimized using Ansoft HFSS. The simulation results of the designed 90° hybrid show that the coupling and isolation are 3 dB and more than 16 dB, respectively. The overall phase difference between the through and coupled ports is $90° \pm 1°$ over the frequency range of 45–75 GHz.

## III. Measurement Results

The die micrograph of the fabricated phase shifter is shown in Fig. 2, where the chip area excluding pads is 0.3 mm × 0.25 mm. Using on-chip measurements with Cascade probes, the phase shifter was tested from 50 to 65 GHz (65 GHz was the maximum frequency of operation of the test setup). The insertion loss versus the control voltage is shown in Fig. 3, for a set of frequencies. With only small changes in insertion loss over frequency, this phase shifter demonstrates approximately 3.5 dB of loss variation across all control voltage values. As discussed in [7] (see Section I) the variation in insertion loss is an intrinsic characteristic of passive or digital phase shifters, but it can be compensated to a large extent by an efficient beamforming algorithm.

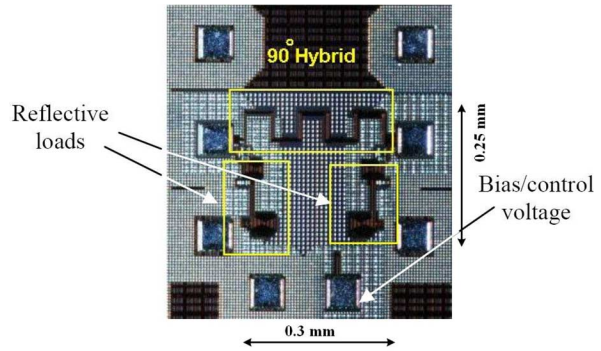


Fig. 2. Die micrograph of the 90 nm CMOS RTPS.

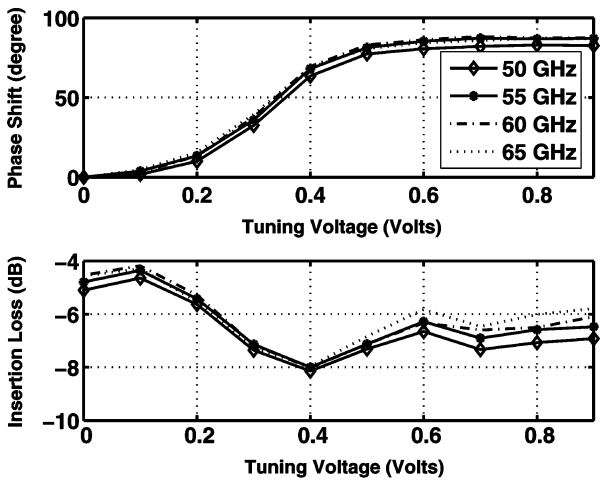


Fig. 3. Measured relative phase shift and insertion loss of the phase shifter versus control voltage at 50, 55, 60 and 65 GHz.

Fig. 4 shows the measured phase-shift of the phase shifter versus frequency for different control voltages. The phase varies linearly over 50–65 GHz frequency range. At each frequency the 90° continuous phase shift is obtained by changing the control voltage.

Fig. 5 depicts the insertion loss and return loss of the phase shifter over the entire bandwidth of 15 GHz. The maximum insertion loss is 8 dB (at 0.4 V control voltage).

The return loss of the phase shifter is more than 12 dB at all phase states. Fig. 6 depicts the measured output power versus input power at 0.4 V control voltage, which verifies the linear performance of the device. Thus, the $\mathrm{P_{1\ dB}}$ point of the developed phase shifter is certainly higher than 4 dBm.

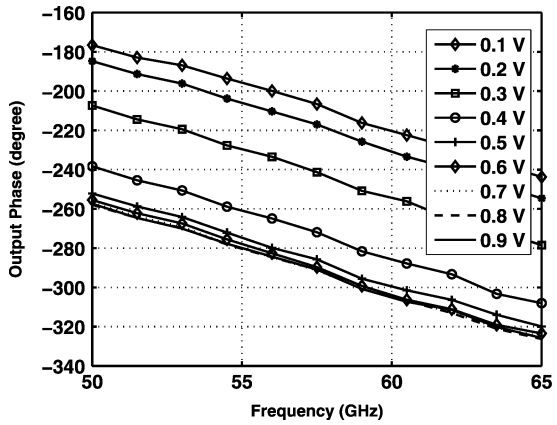


Fig. 4. Measured output phase of the phase shifter versus frequency for various varactor control voltages.

TABLE I
COMPARISON OF THIS WORK WITH OTHER MM-WAVE CMOS PHASE SHIFTERS (VM: VECTOR MODULATION, CONT'S: CONTINUOUS PHASE SHIFT)

| Reference | [2] | [4] | [5] | [6] | This Work |
|---|---|---|---|---|---|
| Technology | CMOS 130 nm | CMOS 65 nm | CMOS 90 nm | CMOS 130 nm | CMOS 90 nm |
| Frequency (GHz) | 15-26 | 55-65 | 40- 75 | 60 | 50-65 |
| Phase shifter type/ Step | VM 4-bit | Digital 4-bit | VM Cont's | VM 4-bit | RTPS/ Cont's |
| Phase shift | 360° | 180° | 360° | 360° | 90° |
| Die Area | 0.14mm$^2$ | 0.2 mm$^2$ | 0.4 mm$^2$ | 0.95 mm$^2$ | 0.08 mm$^2$ |
| Power Consumption | 11.7 mW | ~0 mW | 30 mW | 72 mW | ~0 mW |
| Insertion loss (dB) | 3.5± 2.5 | 9.4± 3.1 | 18 ± 2 | N/A | 6.25 ± 1.75 |

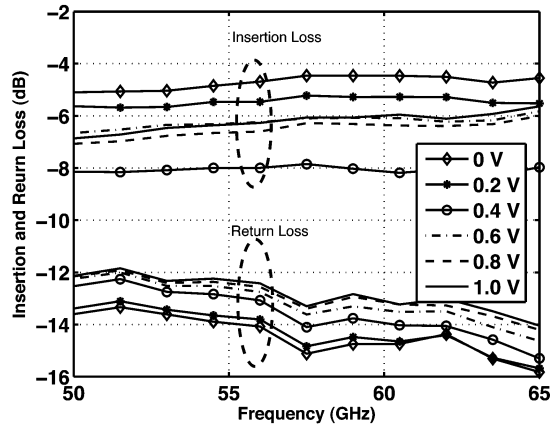


Fig. 5. Measured insertion loss and input return loss of the phase shifter versus frequency for various control voltages.

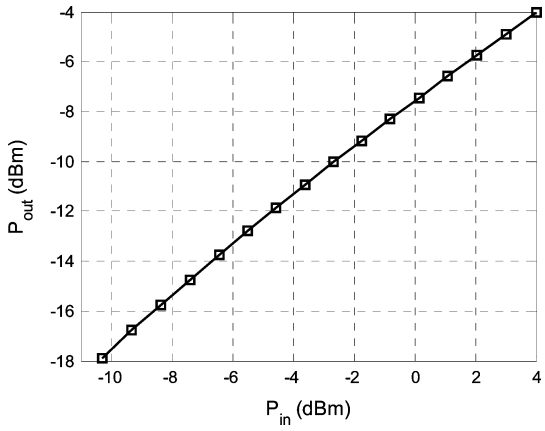


Fig. 6. Measured output power versus input power at 0.4 V control voltage.

## IV. CONCLUSION

A wideband reflective-type phase shifter operating from 50–65 GHz was designed and implemented in 90 nm CMOS technology. The measured results showed that a continuous 90° phase shift over the whole frequency range has been achieved. Moreover, the average insertion loss was close to 6 dB at all phase states. Table I compares this work with other similar works [2], [4]–[6]. This work has the lowest chip area and power consumption.

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