Methods for Failure Analysis and Diagnosis of Millimeter-Wave System-in-Packages

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***Abstract*—This paper presents a sequence of affordable methods applied to diagnose a millimeter-wave system-in-package. The module used in this paper is a 60 GHz transceiver with a waveguide interface, designed to transmit 8 dBm of saturated power. It consists of a flip-chipped RFIC, a multi-layer organic substrate, a metal enclosure with a standard waveguide interface, passive components and a 30-pin connector. The first measured output power was 3 to 6 dB below the desired value over the 60 GHz band. Thus, all parts of the module were thoroughly investigated to detect the cause of power drop. By 3-D electromagnetic simulation of the enclosure, the cavity modes and power leakage in the enclosure were detected, which were verified by measuring the scattering parameters of the back to back configuration. By statistical analysis of the scanning electron microscope images of the cross section of 10 SiP samples, the realized dimensions of the fabricated substrate were measured and applied to the post-fabrication simulation, resulting in a 4 GHz shift in the frequency response. To measure the high frequency performance of the RFIC independent of the enclosure and transition, focused ion beam milling was used to isolate die from waveguide transition, and generate probing pads to directly measure the die output power. Furthermore, the effect of IR-drop, caused by the evaluation board circuits and connector, on the output power as well as the frequency response of the connector were measured. Finally, it is shown that by the full-wave analysis of the layout in HFSS, the resonating traces can be detected and modified to avoid power drop. At the end an algorithm is proposed for the diagnosis and fault detection of mm-wave system-in-packages.**

***Index Terms*—FIB, SEM, 60 GHz, CPW, flip-chip, millimeter wave, waveguide, fault detection, failure analysis, product design, millimeter-wave, system in package.**

I. Introduction

DIAGNOSIS of complex microwave and millimeter-wave (mm-wave) systems is an important step in product design for industrial application, which requires a significant amount of time and money [1]. This is more critical for System-in-Package (SiP) applications, where a high component integration density increases the risk of failure. Yet, no standard algorithm has been defined for micro/mm-wave SiPs diagnosis. Due to the aggressive technology scaling and multi-GHz operating frequencies of radio frequency (RF) devices, parametric failure test and diagnosis of RF circuitry is becoming increasingly important for the reduction of production test cost and faster yield ramp-up [2], [3]. Moreover, the increasing levels of integration and high speeds of operation have made testing complex SiPs very difficult [4], [5].

A System-in-Package is the combination of multiple ICs and components integrated in a module that performs as a system or subsystem. Mm-wave SiPs usually include antennas or waveguide elements to transfer or radiate high frequency signals more efficiently, as printed transmission lines are lossy at this band ($>$ 0.1 dB/mm) [6]. Presence of a radiating element in a densely populated package increases the risk of resonance and power coupling or leakage [7], [8]. Due to the high propagation loss at mm-wave, e.g., 68 dB loss for 1 m range at 60 GHz, every factor which degrades the output power on the SiP side must be carefully investigated and diagnosed to achieve the required range and data rate which usually exceeds 1 Gb/s for mm-wave products [9].

In this paper, we use a practical system, a 60 GHz transceiver module, as a case to introduce and investigate different methods for diagnosis of mm-wave SiPs. The 60 GHz module with a waveguide interface consists of metal enclosure and organic substrate. Measured output power is used as a criterion for performance evaluation. It is convenient to start the diagnosis process from mechanical parts which are easily replaceable and can be modified rapidly. For example, back-to-back measurement is used to identify cavity modes and estimate the overall insertion loss of the metal enclosure. The coexistence of mechanical and electrical parts adds to the complexity of diagnosis procedure, but we show at mm-wave it is possible to import the enclosure CAD model, and substrate layout into powerful electromagnetic (EM) solvers to analyse them simultaneously. Next, we describe methods for diagnosis of the substrate itself, including high resolution imaging of the substrate cross section, flip-chipping bumps and pads, and traces. The statistical analysis of several samples is necessary to determine the fabrication tolerances. The average values for realized dimensions can be used to modify the initial design. This is called the post-fab simulation. Furthermore, to investigate the RFIC performance independent of the SiP, the Focused Ion Beam (FIB) milling is used to isolate die from SiP. Then, the die output power is measured directly with calibrated GSG probes and compared with simulated value. Finally, we show the evaluation-board can have a significant contribution in the overall output power drop, due to the IR

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drop in the board and limited bandwidth of the connectors. One goal of this paper is to focus on the affordable and relatively fast diagnosis methods for researchers and small-size companies.

The organization of the paper is as follows. Section II briefly explains the 60 GHz waveguide module structure. Section III describes the first measured results. Section IV discusses the metal enclosure diagnosis process. Section V explores SiP diagnosis process. Section VI shows how FIB milling is used to measure the RF power of the 60 GHz die. Section VII tackles the evaluation board diagnosis methods, and finally Section VIII concludes this paper.

II. Waveguide Module Design for Backhaul Applications

The SiP studied in this work is a 60 GHz transceiver system with a standard waveguide interface, known as WR-15. Use of mm-wave carriers for backhaul and point-to-point application is rapidly growing due to the demands for higher data rates [10]. At 60 GHz the electromagnetic waves decay significantly due to the physical barriers, such as humans (10−20 dB attenuation [11]), walls, oxygen absorption (15 dB/km at sea level), and water vapour absorption (12 dB/km for 30 mm/hr rainfall). Thus, high gain antennas, such as dish or horn antennas, are necessary for relatively long range applications, which usually have a waveguide input [12]. It clarifies why a 60 GHz transceiver with waveguide interface is required. The designed waveguide module consists of a microstrip to waveguide transition, a 4-layer package with a flip-chipped 60 GHz RFIC, passive components, a connector, and metal enclosure. In the rest of this paper, *module* refers to the whole device, and *SiP* refers to the device without metal enclosure.

A. Microstrip to Waveguide Transition Design

Fig. 1(a) displays the waveguide transition configuration. The transition design details are beyond the scope of this paper and can be found in [13] and [14], so only a brief structure review is presented here. The transition is a double tapered microstrip line to rectangular waveguide (WR-15) transition implemented in a four-layer substrate discussed in Section II-B. The microstrip line on the top metal layer is tapered at die side to smoothly match the die pitch to 50 Ω line-width. The top ground section is connected to the bottom ground through via fences forming a semi-rectangular dielectric waveguide inside the substrate shorted on the bottom. Part of this transition is a metal waveguide mounted on top of the substrate. The step-tapered end of the microstrip line is extended to the dielectric waveguide region acting as a current source inside the waveguide, which excites the waveguide modes. Fig. 1(b) shows the scattering parameters of this transition. The 10-dB impedance bandwidth (S_{11}) is 14.3 GHz ranging from 53.3 to 67.6 GHz (or 24% fractional bandwidth). The insertion loss (S_{12}), varying from 0.3 to 0.8 dB over the 14 GHz bandwidth, rolls off at higher frequencies ($f \geq 68$ GHz). The dielectric constant and loss tangent of the substrate at 60 GHz are 3.3 and 0.0035, respectively.

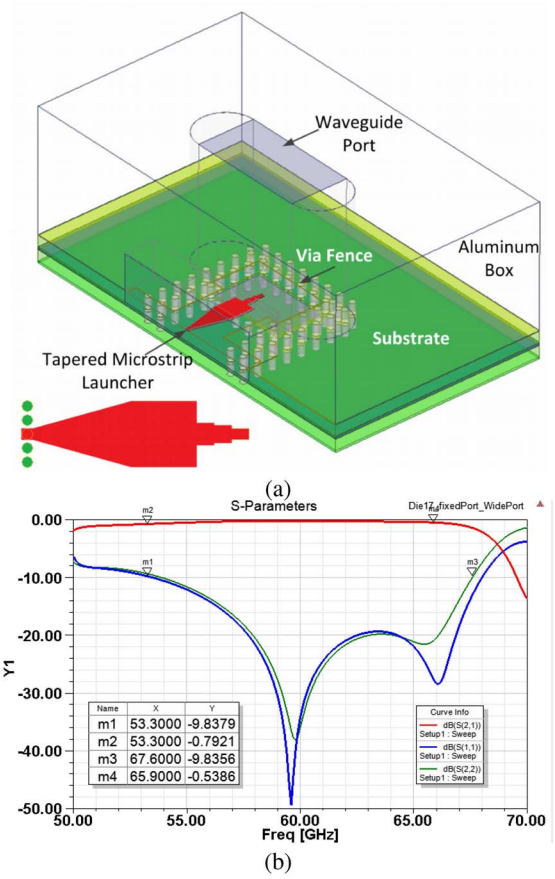


Fig. 1. (a) Microstrip to waveguide transition model. (b) Simulated S-parameters in HFSS, from 50 to 70 GHz.

B. SiP Design and Fabrication

Amongst different IC packaging technologies, substrate technology offers more aggressive design rules. For example, trace width and spacing in substrate technology can be as low as 15 μm, whereas in PCB technology the lower limit is 75 or 100 μm. Thus, substrate technology allows for a denser routing, and possibly smaller package size and cost. The cost depends on multiple factors such as, volume, number of layers, package size, variety of via-holes and surface finish.

The 60 GHz RFIC used in this work is a transceiver with a size of 2.1 × 2.1 mm^2 implemented in SiGe technology, designed for a saturated output power (P_{SAT}) of 9 dBm over 60 GHz band (57-66 GHz) [15]. It has 77 bumps with 160 μm pitch. There are two separate bumps for TX and RX signals with 1.9 mm spacing. Based on the number and function of die input/output pads a minimum of four metal layers is required to design a waveguide-interface SiP.

Fig. 2(a) shows the top layer of the designed SiP layout, where die is flip-chipped to, and TX and RX waveguide launchers are located. By flip-chipping die to the top layer the shortest traveling distance for 60 GHz signal is achieved without any via interconnect in 60 GHz signal path. Since the transmitter and receiver RF pads are on two opposite sides of the die, two identical microstrip to waveguide transitions are implemented in this SiP for TX and RX functions. Fig. 2(b) demonstrates the symmetric 4 metal-layer stack-up

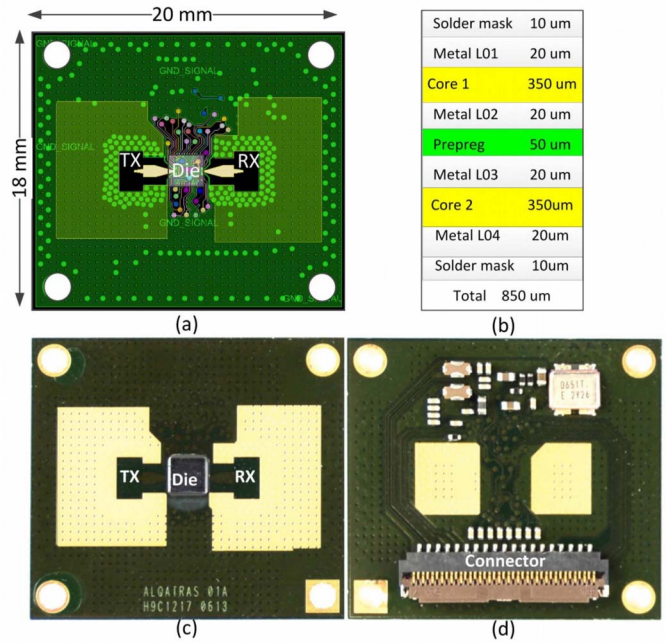


Fig. 2. Designed and fabricated SiP. (a) Top layer of the SiP layout, (b) substrate stack-up, (c) top view of the fabricated SiP showing the flip-chipped die, and (d) bottom view. The shiny regions show the exposed ground sections.

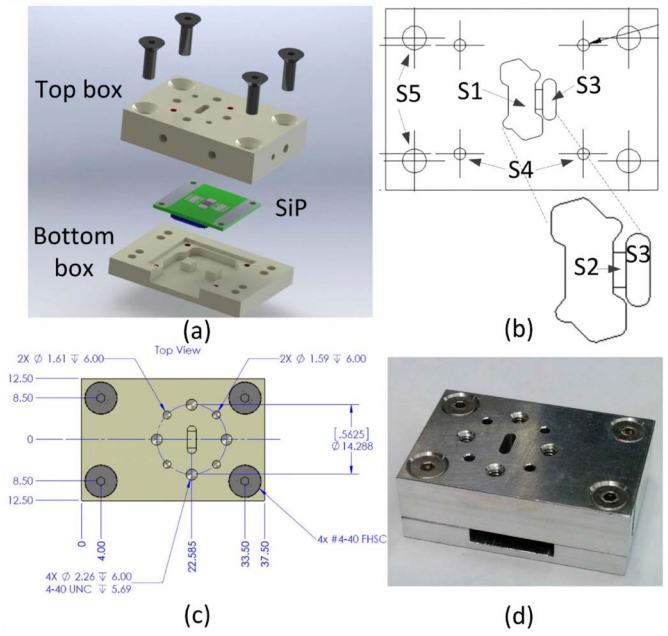


Fig. 3. Metal enclosure design for die to waveguide transition, (a) 3D exploded view, (b) cavity inside the top box, (c) top box dimensions, and (d) fabricated box.

used to design this SiP, which consists of two dielectric cores of 350 μm thickness and a 60 μm bond layer (prepeg) in between. A thin layer of solder-mask (SM) resist (10 μm) is placed on all outer traces for isolation and protection purposes. Fig. 2(c) displays the top view of the fabricated SiP showing the flip-chipped 60 GHz die at the center. Fig. 2(d) shows the bottom view of the fabricated SiP, where connector, crystal oscillator and other components are assembled. All components except die are assembled to the bottom side to leave a flat surface on top. The connector facilitates the connection of SiP to external boards and devices. Certain metal regions on the top and bottom ground planes are exposed to allow for electric contact between the metal enclosure and SiP. This SiP design includes 314 Through Hole Vias (THV), 14 blind vias from L03 to L04, and 156 traces on top and bottom layers. The SiP size is 20×18 mm^2.

C. Metal Enclosure Design

Metal enclosure is part of the waveguide transition design. Besides, it is used to hold the external high-gain antenna, and protect SiP. The external antennas with a standard WR-15 flange is assembled to the top of the enclosure. Fig. 3 shows the 3D exploded view of the designed metal enclosure consisting of top and bottom parts. The 60 GHz SiP is sandwiched between these two parts. There is a cavity in the top part shown in Fig. 3(b) to protect the die and microstrip launcher, labeled as S_1. In Fig. 3(b), S_2 is a tunnel connected to waveguide hole denoted by S_3, which protects the microstrip launcher. The waveguide hole has round corners to lower the machining cost, but its width is 1.88 mm according to WR-15 flange specification [16]. Four pins (S_4) are used to place SiP in the right position within the box. Moreover, 4 screw holes (S_5) are used to connect the top and bottom parts. Fig. 3(c) shows the standard WR-15 waveguide flange implemented in the top section. Fig. 3(d) shows a fabricated sample in aluminum with Nickel plating used for surface finish. The final box size is $37.5 \times 25 mm^2$. An opening in the bottom part provides access to SiP connector through a ribbon cable.

TABLE I
BOX VARIANTS SPECIFICATIONS

Box Name	Waveguide Hole	S_1 Depth	S_2 Depth	Contacts)
F_0	Round	1400 μm	600 μm	1/25μm
F_1	Precise	600μm	350 μm	1/25μm
F_2	Precise	600μm	350 μm	2/25μm
F_3	Precise	1000 μm	350 μm	2/100μm
F_4	Precise	1400 μm	600μm	1/25μm
F_5	Round	1400 μm	600 μm	0

1) Box Variants: Several boxes with slightly different features are designed, to lower the internal resonance risk. Table I summarizes the fabricated box variants, which are different in waveguide channel, die-cavity size, S_1, tunnel depth, S_2, or number of contact islands. A contact island is used to touch an exposed region of the SiP for better ground connectivity. A precise waveguide channel is the one without round corners, i.e., the waveguide hole is a rectangle with $3.76 \times 1.88 mm^2$ size.

2) Reconfigurable Box Design: The metal enclosure has only one waveguide channel, but the SiP has two transitions for TX and RX, respectively. The box has a symmetric design, such that by rotating the top part by 180° the waveguide hole is aligned with the other launcher. The motivation behind this design is that the 60 GHz die is a Time Division Duplex (TDD) transceiver, so TX and RX cannot work at the same time.

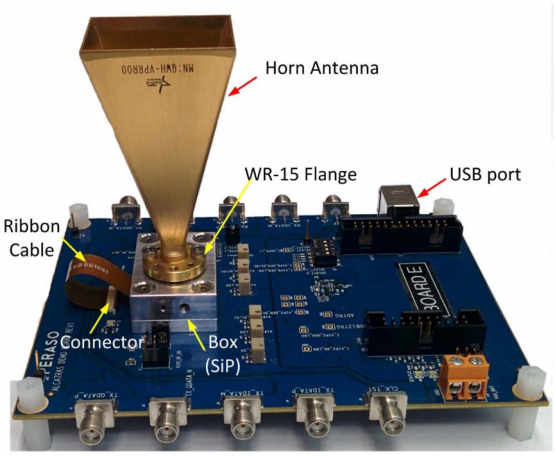


Fig. 4. SiP evaluation board with a pyramidal horn antenna assembled to the module.

D. Evaluation Board Design

Fig. 4 shows the SiP evaluation board with a 24 dBi gain horn antenna assembled to the standard WR-15 waveguide flange of the module. The board is powered up and controlled using a USB cable. The bottom section of the metal enclosure is screwed to the board. The 60 GHz SiP interfaces with the evaluation board through a ribbon cable. The SMA connectors on both sides of the evaluation board are used to exchange baseband data between SiP and external baseband system. For direct power measurement a power sensor with waveguide input is connected to the box, replacing the horn antenna in Fig. 4. A waveguide interface facilitates the silicon measurement significantly if the transition loss is negligible. For example, direct output power measurement with power meter is much simpler than on-wafer measurement with probes, and more accurate than extracting the transmitted power from over the air (link) measurements.

III. First Power Measurement Results

The first test to evaluate the performance of the module, is measuring the output power of the module directly using a waveguide power sensor (V8486A). The output power of the 60 GHz die was not measured directly before this experiment, so simulated values are used to compare the module performance. The simulated saturated power (P_{SAT}) of the die shown in Fig. 5 varies from 7.2 to 9.2 dBm over the frequency. It is assumed that the transmitter output is matched to 50 Ω load. Besides, the insertion loss of the transition is not included in this curve.

A. Measured Power With Different Boxes

Fig. 5 shows the measured output power over frequency for five different boxes described in Table I. The first results were quite disappointing, showing an insertion loss of 3 to 8 dB versus frequency compared to simulated P_{SAT}. Despite differences in metal boxes, all measurements follow a similar pattern from 58 to 61 GHz. Three boxes, F_1, F_2, and F_3, show almost identical behavior. Besides, their performance is worse than the other two boxes at higher frequencies, with

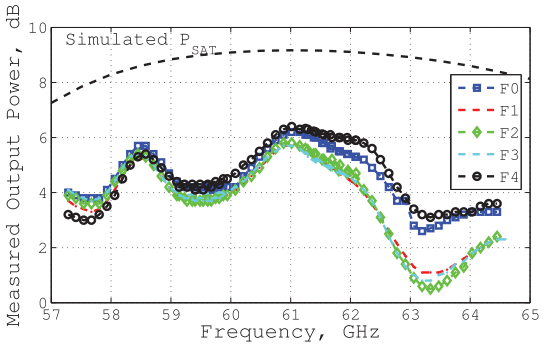


Fig. 5. TX output power of different boxes compared with simulated saturated power of the die.

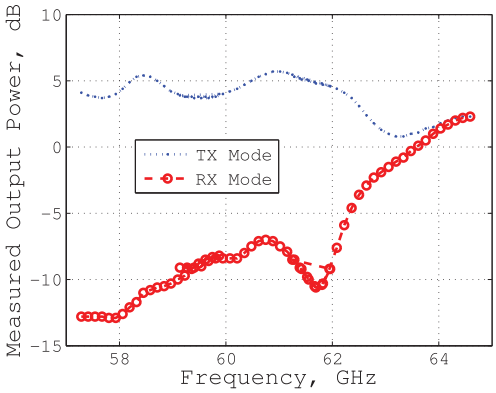


Fig. 6. Measured TX transmitted power and power leakage to RX port.

2 dB extra loss. All these three boxes have smaller tunnel and cavity depths compared to the other boxes.

B. Identification of Problems

Comparing the simulated transition performance shown in Fig. 1(b) and simulated P_{SAT} with the measured output power, three problems are observed:

1) power roll-off at high frequency ($f \geq 62$ GHz)
2) 2 dB ripples from 58 to 61 GHz
3) 2-5 dB extra loss in measured power.

The rest of this paper describes methods and experiments applied to understand the causes of the above problems.

C. Transmitter Power Leakage

One hypothesis is that part of the die transmitter power couples to the RX side of the SiP through the cavity in the top metal box, or substrate. To investigate this hypothesis, a new measurements was performed. The box was assembled in RX configuration, but the transmitter was turned on and LO frequency was swept. The TX power leakage was measured through the RX side with power meter connected to the box. Fig. 6 compares the measured results for this configuration labeled as *RX Mode* with the regular *TX Mode* measurement. As the frequency increases ($f \geq 62$ GHz) the power leakage enlarges, such that at 65 GHz almost half of the output power is coupled to the RX port through the die cavity or substrate. This can explain the power roll-off in Fig. 5.

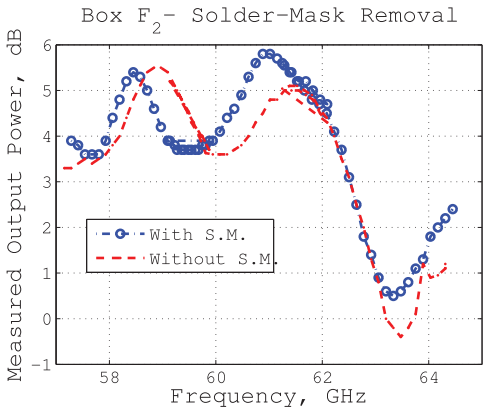


Fig. 7. Effect of solder-mask removal on the measured output power.

D. Solder-Mask Resist Effect

The second hypothesis is that some of the insertion loss is caused by the solder-mask resist(SM) layer on top of the microstrip line, which was not accurately modeled in design process since the 60 GHz dielectric characteristic of the SM resist was not available. To verify this assumption the SM layer on TX transition was removed manually. Fig. 7 shows the measured output power before and after the solder-mask removal. Around 1 GHz of right shift after SM layer removal is observed, but the peak measured power does not change significantly. During SM removal the copper layer was scratched, which might have affected the measured results; however, there is no strong evidence to prove that SM layer has a large contribution in the overall insertion loss. Further experiments revealed that SM loss is lower than the conventional Electroless Nickel Immersion Gold (ENIG) surface plating at mm-wave band.

IV. Metal Enclosure Diagnosis Process

In the previous section the cause of roll-off in measured power at frequencies higher than 62 GHz was revealed, but the reason of 2-5 dB extra insertion loss is not clear. In this section the focus is on exploring box contribution in the overall module loss and ideas to redesign the metal enclosure.

A. Simultaneous Analysis of BOX and SiP

During module design process, transition, SiP and metal enclosure were designed separately with different CAD tools. The microstrip to waveguide transition was designed in HFSS, SiP was designed in Allegro Package Designer, and metal enclosure was designed in SolidWorks. Although some assumptions were made to assure good coexistence of SiP and box, early measured results showed that the integrated solution is far from the desired performance. To analyze the box and SiP simultaneously, some software tools, such as Ansys Alinks for EDA [17] and Workbench Platform [18], were used to import the 3D box model and SiP layout into HFSS. The simulation time is relatively long without model simplification. Similarly, due to the relatively large size of the device, more than a million tetrahedral meshes are generated, which can cause memory shortage and possible crashing.

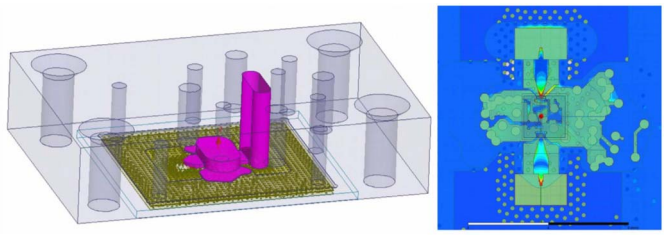


Fig. 8. Importing CAD model of the box and SiP layout in HFSS. The cavity in the box is highlighted. The power leakage through cavity, shown on right, is verified by EM simulation.

Fig. 8(a) shows the full model generated in HFSS. In the first iteration of full-wave analysis the narrow traces were not included and a hexagonal model was used for vias. Fig. 8(b) displays E-field magnitude at 65 GHz, while TX side is excited. It is seen that TX signal couples to RX side through box cavity, with almost equal magnitude, which is in full agreement with measured results in Fig. 6. Now that we have confidence in simulation benchmark, we can explore the die-cavity behavior more precisely.

B. Back-to-Back Box Configuration Modeling and Measurement

One hypothesis to explain the ripples in measured output power is that there is a resonance in the box-SiP configuration, which sucks energy from the direct channel. Because of the complex shape of the cavity, shown in Fig. 3, it is not possible to calculate the resonant modes analytically, but it is possible to measure a back-to-back configuration of two top metal boxes. First, we used our simulation tools to see if such resonance for a back-to-back configuration exists. Fig. 9(a) and (b) show the E-field magnitude at 57 GHz and 61 GHz, respectively. In this simulation two identical top metal enclosures F_2 are connected from the cavity size, forming a long waveguide channel and a die cavity twice larger in size. It is seen that at 57 GHz a large amount of the input power couples to the die cavity, which is resonating, and reflects back to the input port, whereas at 61 GHz a negligible amount of the input powers couple to the die cavity. Fig. 9(c) shows the simulated insertion loss of the long waveguide channel, illustrating that the cavity behaves like a filter from 56 to 60 GHz. There is a null at 56.6 GHz and some ripples over the frequency band.

To verify the cavity filtering behavior, a series of back-to-back measurements were conducted. Fig. 10 shows the measured insertion loss for three different back-to-back configurations:

- $F_2 - F_4$ cavity height 2000μm
- $F_1 - F_2$ cavity height 1200μm (one contact)
- $F_4 - F_4$ cavity height 2800μm

In all cases a resonance is seen between 57 to 59 GHz. Although the total cavity height changes from 1200 to 2800 μm the resonance frequency does not change significantly These measurements can verify the reason of insertion loss at lower 60 GHz band.

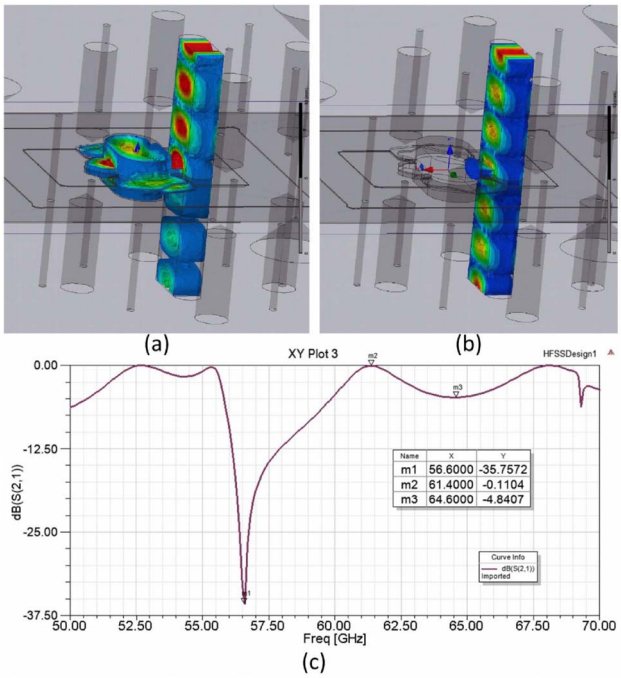


Fig. 9. Simulated results of the back-to-back metal box configuration. (a) Electric Field magnitude at 57 GHz. (b) Electric Field magnitude at 61 GHz. (c) Insertion loss from 50 to 70 GHz.

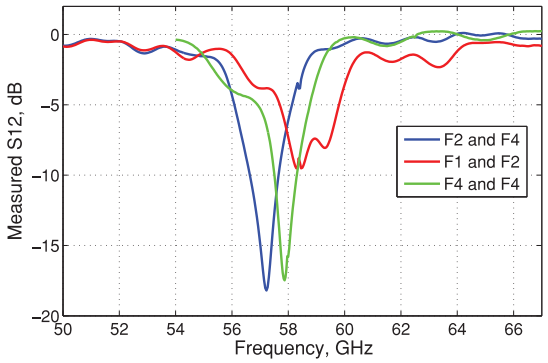


Fig. 10. Measured insertion loss of three different top metal enclosure back-to-back configuration.

C. Top Enclosure Redesign With Open Cavity

Previous analysis proved the existence of cavity modes in the top metal. But in practice SiP is inside the box. Interaction of die, SiP and box is a complicated problem. The current SiP design does not allow a simultaneous two port measurement to investigate the cavity mode, because the spacing between two launchers is very short. So a new box was designed with a cut at the middle to remove the closed cavity shown in fig. 3(b). Fig. 11 shows the new box, named F_8, and compares the measured output power of this box and a box with cavity (F_0). It is seen that the ripple between 58 and 61 GHz is gone. In one measurement the open cavity was filled with a small piece of absorber, which shows a higher output level. The primary idea of placing the absorber was to block the wave leakage through microstrip channel, denoted by $S2$ in fig. 3(b). At high frequency this new box has a worse performance which

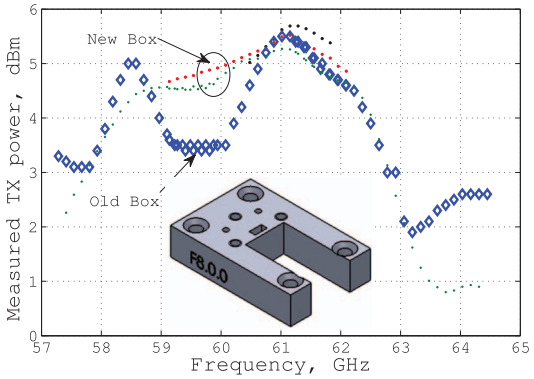


Fig. 11. Measured output power of the new box. The inset shows new box.

is due to the high-precision waveguide channel as seen before in Fig. 5.

V. SiP Diagnosis Process

In the previous Section, the causes of two problems of the module, i.e., roll-off in the measured power and ripples in band were discovered, but still the high insertion loss of the module is not justified. For example, back-to-back measurements in Fig. 10 show that there are some frequency slots where the box is nearly loss-less (e.g., $f \geq 61$ GHz), where as in Fig. 5 a minimum 3 dB loss is observed. To understand the source of this loss we need to put one step forward and analyse the SiP structure and performance in details. We investigate methods to verify fabricated SiP stack-up, statistical analysis of fabricated samples, and more full-model simulations.

A. Scanning Electron Microscope (SEM) Imaging

SEM imaging is often used in semiconductor technology to provide a detailed and high resolution view of silicon. In this work, SEM imaging was used to measure the precise cross section and top/bottom view of the fabricated substrate. Fig. 12(a) shows the two cross sections of the SiP defined for SEM imaging, namely CS1 and CS2. The first cross section, CS1, passes through the die and the symmetry access of the SiP. The second one, CS2, cuts a via fence. Fig. 12(b) shows the SEM image of CS1, showing silicon die, bump, microstrip transition, and ground planes. Fig. 12(c) shows a high resolution image of the solder bump in the flip-chipped die, which carries mm-wave signal. Fig. 12(d) shows the SEM image of the tapered microstrip line and the solder-mask on top. The first impression is that SiP fabrication is free of major faults, all metal layers are flat, die flip-chipping has no issue, and vias have equal sizes.

Fig. 13 shows a closer look at CS2, displaying the stack-up and two adjacent THVs with dimensions measured using calibrated imaging tools. Each dielectric layer is 20 to 30 μm thicker than the design values indicated in Fig. 2(b). Moreover, the solder-mask layer is 20 μm thick. So, the total thickness is 920 μm compared to 850 μm used in pre-fab design. Although this deviation is within the 10% fabrication tolerance specified by the supplier, it causes 4 GHz left shift in S-parameters and up to 2 dB increase in insertion loss as seen in Fig. 13(c).

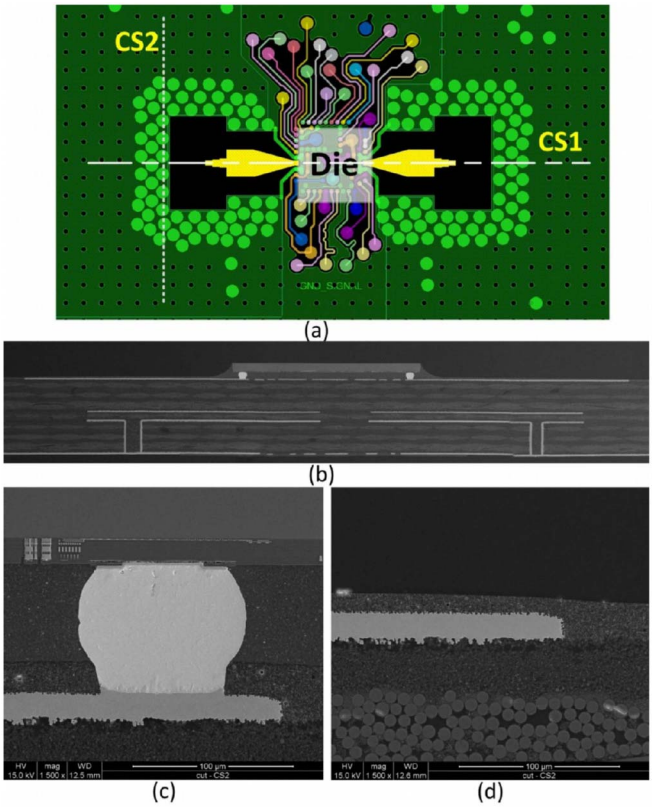


Fig. 12. Scanning Electron Microscope (SEM) Imaging of the SiP. (a) Definition of the two cross sections (CS1, CS2), (b) CS1 SEM image, (c) SEM image of a flip-chipped solder bump, and (d) solder mask on top metal layer. solder mask.

TABLE II
STATISTICAL DATA OF 10 SIP SAMPLES EXTRACTED FROM SEM IMAGING

Parameter	Min (μm)	Max (μm)	Mean (μm)	STD (μm)
Top SM	17	18	18	0.5
L1 Cu Thickness	17	24	21	3
Core 1 Thickness	370	375	372	2
L2 Cu Thickness	18	20	19	1
Prepreg Thickness	78	82	80	2
L3 Cu Thickness	19	24	21	2
Core 2 Thickness	370	375	372	2
L4 Cu Thickness	18	22	20	1
Bottom SM	17	18	18	0.5
Ni (ENEPIG)	5.8	6.6	6.2	0.27
Au (ENEPIG)	0.055	0.058	0.056	0.001
Pd (ENEPIG)	0.067	0.078	0.070	0.003
SiP Thickness	923	929	926	2.5

B. Statistical Analysis of Fabricated SiP Dimensions

To understand the fabrication tolerances and sample variation, the dimensions of 10 samples were measured. The statistical analysis results are given in Table II. The small standard deviation (STD) of the measured dimensions indicate that the fabrication tolerance is negligible, which is a significant advantage of substrate technology. Similar analysis is applied to trace width and via size. The mean trace width is $33 \pm 1 \mu$m. The average outer via diameter is $203 \pm 3 \mu$m.

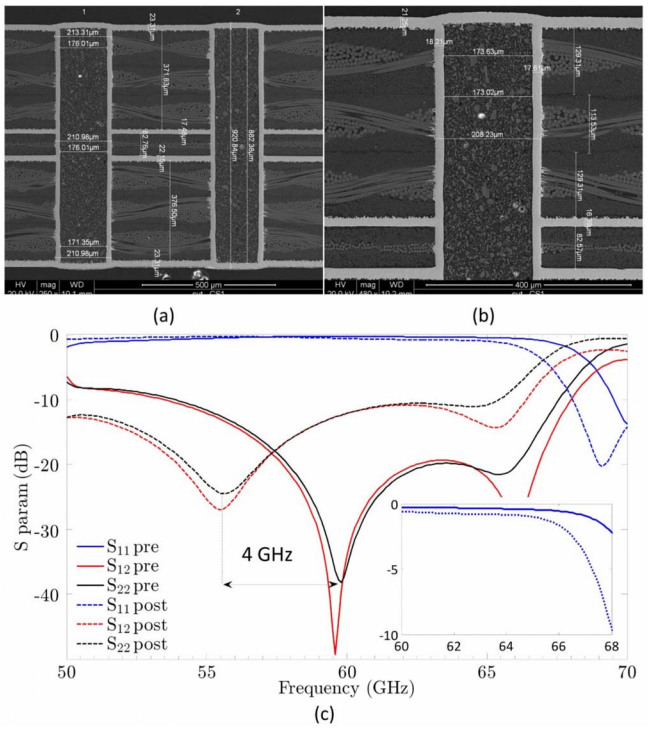


Fig. 13. Post-fab analysis of SiP. (a) SEM image of SiP cross section. (b) Zoomed view of SiP cross section showing core and prepreg layers. (c) Comparison of pre-fab and post-fab simulated S-parameters. The inset shows the pre/post-fab simulated insertion loss.

SEM imaging facilitates the measurement of surface finish layers of the fabricated SiP, which are as thin as 50 nm. The statistical data for metal plating (surface finish) is summarized in Table II. In this work, Electroless Nickel/ Electroless Palladium / Immersion Gold (ENEPIG) is used, which has excellent solderability for lead-free Sn-Ag bumps used in die flip-chipping [19]. On the other hand, the relatively thick layer of Electroless Nickel, with poor conductivity, increases the insertion loss of the 60 GHz microstrip lines.

C. Layout Redesign

In package design, the via-pad size is usually twice the via diameter, which is itself proportional to the dielectric core thickness. In this design, where core thickness and via size are 350 and 200 μm, respectively, the via-pad size is 350 μm. This affects minimum via-spacing (450 μm). On the other hand, 60 GHz die and connector are assembled to the opposite sides of the SiP, so multiple vias are required to route I/O signals. Consequently, the traces from die to via-pad on top layer become meandered and relatively long as seen in Fig. 12(a). These traces are very close to high frequency signal paths. During full-model simulation of module, it was noticed that some of the traces are resonating. It was experimentally verified by the open-box experiment in Fig. 11, when by scanning a piece of absorber on different traces the measured power level changed. To understand the cause of package resonances, a series of full-model simulations are executed in HFSS.

Fig. 14(a) shows a section of the original SiP layout under die, between two transitions, where the trace density is high.

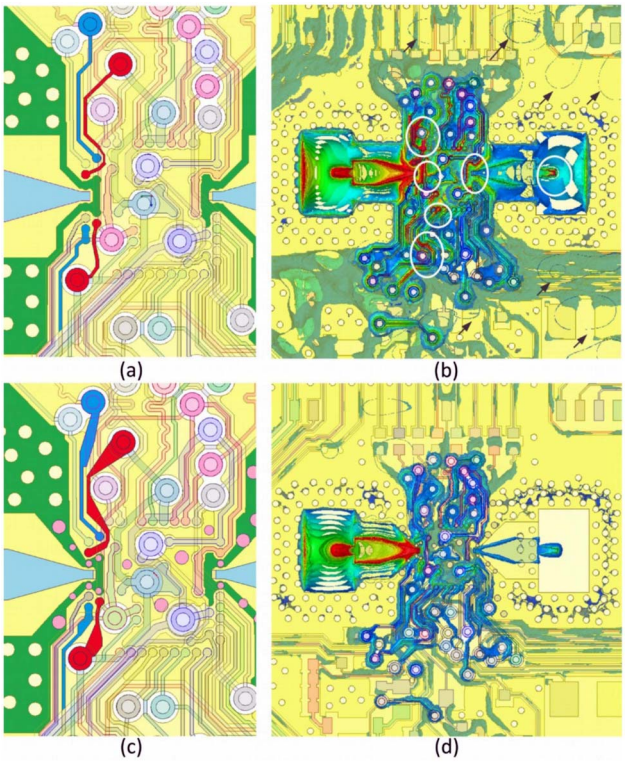


Fig. 14. Magnitude of E-field in top dielectric layer.

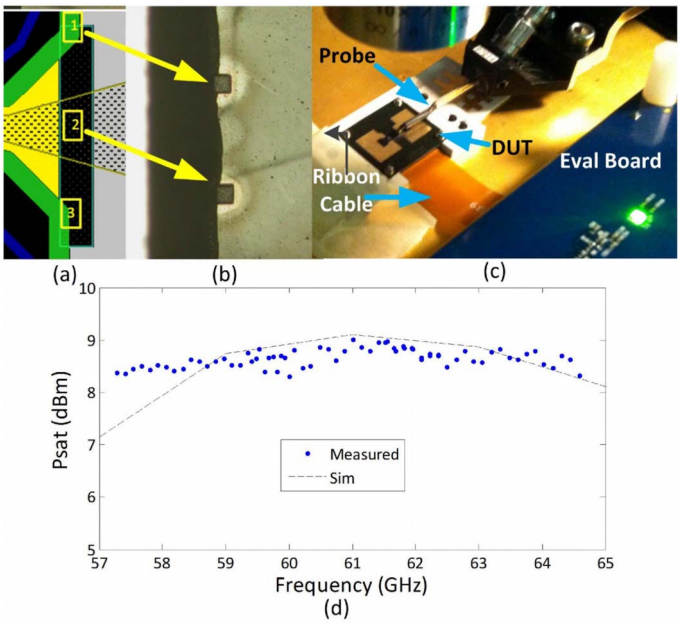


Fig. 15. Focused Ion Beam Sectioning. (a) Desired probe pad locations, (b) Realized pads with FIB, (c) measurement set-up, and (d) Measured output power of die.

Fig. 14(b) shows the intensity of Electric Field in top dielectric layer, when TX transition (left) is excited. The white circles highlight the regions where an undesired high field density is observed. The black arrows show local in-SiP resonances. It is seen that three traces highlighted in Fig. 14(a) with blue and red colors, are coupled to TX transition. Moreover, E-field is coupled from the TX transition to the RX transition as seen before. After identifying the resonating traces, the layout is modified to avoid such resonances (Fig. 14(c)). The resonating traces are widened as much as possible. Particularly, the via-pads are filleted. The ground regions around die-transition are widened and tapered smoothly to open room for more ground THVs. Besides, a few THVs are added in ground islands between TX and RX transitions. Based on extensive simulations, a narrower THV structure with 100 μm diameter is defined and placed in narrow ground strips around TX and RX bumps, where there is no room to widen the ground regions or place regular THV (200 μm diameter). This is a violation of the current design rules, but shows the approach which must be taken in SiP redesign. Finally, Fig. 14(d) illustrates the E-field intensity in the modified SiP. The field is completely confined in the transition region and the in-SiP resonances are diminished.

VI. 60 GHz Die Diagnosis

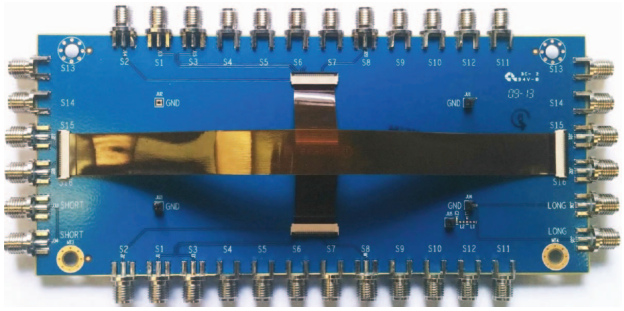
Focused Ion Beam (FIB) milling is used as a method to repair and diagnose ICs [20]. FIB systems use a finely focused beam of ions that can be operated at low beam currents for imaging, or high beam currents for site-specific sputtering or milling [21]. The purpose of this Section is to explore the capability of FIB milling as a tool for diagnosis of a SiP.

A. Focused Ion Beam Sectioning

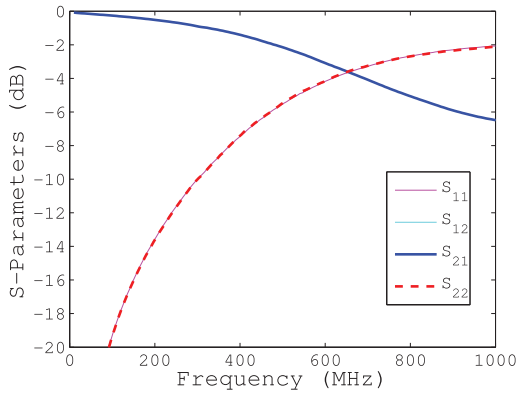
As mentioned in Section III, die output power was not measured directly before and simulated values for P_{SAT} were used to calculate module loss. By probing the die TX pad from package side, we are able to measure the TX output power and have a better estimation of module loss. To accomplish this goal, die must be disconnected from microstrip transition, and ground-signal-ground (GSG) pads must be formed for probing. /Using FIB milling a gap is created in TX transition, which cuts it from the flip-chipped die. Besides, the SM resist on the remaining part of the tapered microstrip line connected to die TX side, is etched to open three pads for GSG probing. Fig. 15(a) and (b) show the desired and realized pads for 450 μm pitch GSG probing. The pad size is 50$\mu m\times$ 50μm. The dark region on the left side of Fig. 15(b) shows the area covered by underfill, which is extended to 500 μm out of die. Probing pads must be as close as possible to die to lower the insertion loss. The signal pad in Fig. 15(b) is slightly off from the desired position, but close enough to land probe.

B. Measured Die Output Power

Fig. 15(c) shows how the fibbed sample is probed in a probe station. The exposed sample is held on the bottom box and a ribbon cable connects the SiP to the evaluation board. Fig. 15(d) shows the measured saturated power P_{SAT} of the transmitter versus frequency. It is seen that P_{SAT} hovers between 8 dBm to 9 dBm over frequency. This is close to the design value of 10 dBm, and proves that SiP is not the major source of loss in this design.



(a)



(b)

Fig. 16. Evaluation of the RF performance of the ribbon cable and connectors. (a) Test-board. (b) Measured S-parameters.

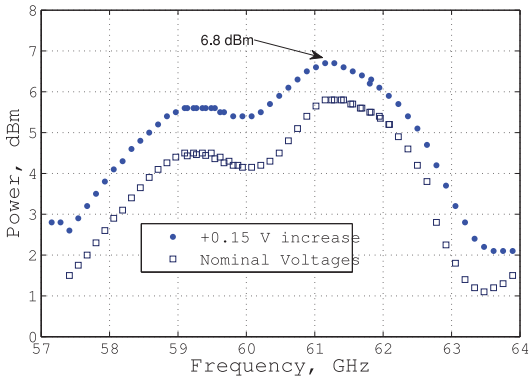


Fig. 17. Measured output power before and after IR-drop compensation.

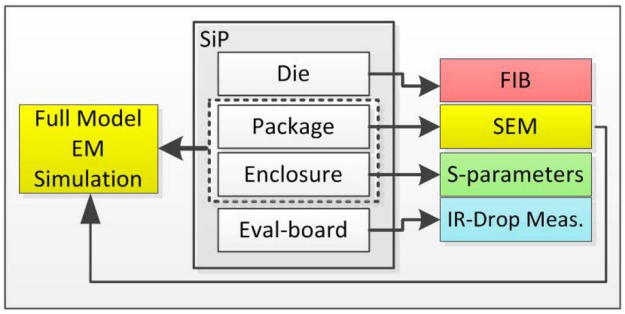


Fig. 18. Methods for diagnosis of a mm-wave system in package.

C. De-Embedding Probe Loss

The most challenging part in extracting the output power is calculating the probe loss. Two probes of the same type were landed on a true line in the ceramic probe calibration kit provided by the probe supplier. The S_{21} of the cascaded probes was measured and divided by 2 to obtain individual probe loss.

VII. Board Level Diagnosis

The evaluation board described in Section II-D provides biasing, filtering and control signals. Initially, the board goes under a sanity check, which usually includes DC measurements, process to makes sure it is functional; however, the impact of the board, particularly connectors and ribbon cable, on RF performance of the module needs to be investigated.

A. RF Performance of Ribbon Cable and Connector

To evaluate the RF performance of the ribbon cable and connector, a test board is developed shown in Fig. 16(a). There are two ribbon cables with different lengths (2 and 6 inches). Both ends of each cable are connected to the same type of connectors used in eval-boards. Certain connector pins are connected to SMA connectors to measure impedance matching, insertion loss and cross coupling of single and differential lines in ribbon cable. Fig. 16(b) shows the measured S_{11} and S_{12} of a single line on the short ribbon cable. It is seen that as frequency increases the insertion loss increases significantly due to the poor matching. So, use of such ribbon cable to carry frequencies higher than 300 MHz is not recommended. In this 60 GHz RFIC I/Q data lines can carry up to 900 MHz signal.

B. IR Drop Compensation

Another observation from SiP measurements was that the sensors inside the die show the bias voltages are smaller than the nominal values, implying a possible voltage drop in eval-board. It was confirmed by DC measurements that the ohmic loss of the bias path from external power supply to the die causes up to 0.15 V drop, known as IR drop [22]. Using variable resistors in eval-board this drop was compensated. Fig. 17 shows the measured output power before and after voltage drop compensation. The module output power increases by 1 to 1.2 dB after IR drop compensation.

VIII. Conclusion

Several methods were used to diagnose a micro/millimeter-wave SiP, which consists of a high frequency die integrated in a multi-layer package, metal enclosure and evaluation board. Fig. 18 shows the proposed diagnosis flowchart. The highlights of this work are as follows.

- SEM imaging can be used to analyze the inside of the package, and compare the realized dimensions with the design values. The statistical analysis of the dimensions of multiple SiPs is highly recommended to understand the fabrication tolerances. Post-fabrication simulation using realized dimensions, can justify the cause of some issues such as shift in frequency response and roll-off in measured parameters.

- Measuring s-parameters of the enclosure with or without SiP can reveal the possible resonances, and power leakage.
- FIB milling helps to separate die from package and measure ite]s performance independent of package or enclosure effects.
- The evaluation board, used to drive the SiP, can degrade the module performance by IR drop or limiting the frequency response.
- Full-wave EM simulation of the SiP and enclosure (or at least SiP itself) provides a lot of helpful information to diagnose the module and modify the design.
- Particularly, in this work it was shown that narrow vias and wide or tapered traces improve the performance of the mm-wave SiP. It is better to avoid cavities in the enclosure, for example by placing die on the opposite side of the waveguide flange. Cavities in the enclosure increase coupling between TX and RX sections.

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