A 60 GHz, 802.11ad/WiGig-Compliant Transceiver for Infrastructure and Mobile Applications in 130 nm SiGe BiCMOS

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***Abstract*—A fully integrated 802.11ad/WiGig compliant 60 GHz transceiver is presented in a 130 nm SiGe BiCMOS technology. Encompassing an area of 2.3 mm $\times$ 2.16 mm $=$ 4.97 mm^2, the transceiver covers the entire 60 GHz band, from 57 to 66 GHz. Within this span, the RX NF, TX OP1dB, and PLL RMS jitter is better than 5.5 dB, $+$13.5 dBm, and 7°, respectively. The transceiver is packaged in 1) a system-in-package substrate with industry standard WR-15 transition providing an approximate 1 dB insertion loss, and 2) a cost-effective 7 $\times$ 7 mm^2 organic BGA package with integrated transmit and receive antennas providing 8 dBi gain. In system-level testing, the transceiver is fully compliant with all TX EVM and RX sensitivity requirements of the WiGig standard up to the top-rate 16-QAM operating mode and across all standard channel frequencies. Link testing over the air with the antenna-integrated package shows a range of 5.9 m at 4.6 Gbps and over 20 m at 2.5 Gbps. This system achieves the highest performance 802.11ad/WiGig compliant wireless links of any reported single-element transceiver.**

***Index Terms*—Antenna-in-package, BiCMOS, IEEE 802.11ad, mm-Wave, radio transceivers, SiGe, 60 GHz, WiGig.**

I. Introduction

THE unlicensed 60 GHz band offers unprecedented access to uninterrupted spectrum that is on the cusp of being fully utilized for a range of applications by both start-ups [1]–[3] and established communication companies [4]–[7]. Many potential applications exist, within both consumer and enterprise sectors, that seek to leverage the high data-rate and low-latency wireless links enabled by this technology. Research into 60 GHz transceiver design, including the optimal tradeoff between performance, area, and cost has been extensive and robust [5], [8]–[16].

The adoption of the Wireless Gigabit Alliance (WiGig) specification by the Wi-Fi Alliance as part of the next-generation Wi-Fi protocol, IEEE 802.11ad-2012 [17], was a major step forward for 60 GHz technology. This demonstrated the industry's readiness to move forward in a unified manner and avoid the potential fragmentation that can occur without a widely accepted industry framework. The IEEE 802.11ad-2012 standard defines up to four 2.16 GHz wide channels with centers at 58.32, 60.48, 62.64, and 64.80 GHz. Signaling schemes up to 16-QAM are supported under single-carrier (SC) operation, or up to 64-QAM with OFDM, delivering peak rates of 4.62 and 6.76 Gbps, respectively. Furthermore, the standard defines beam-forming protocols permitting the use of phased-array transceivers that can enable system performance enhancements at the cost of increased silicon area, package area, and DC power consumption.

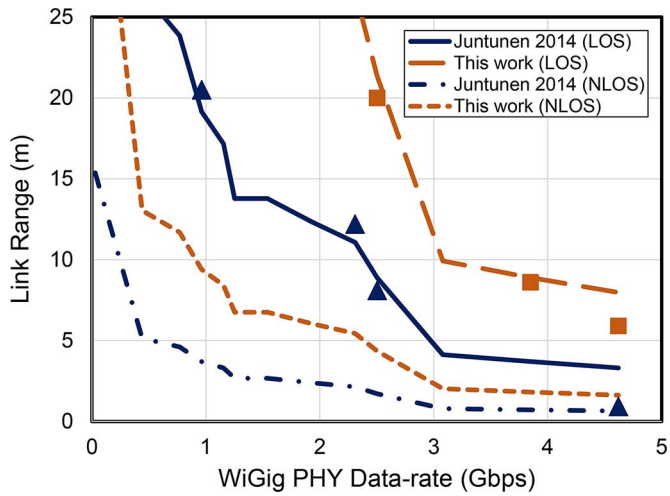

Fig. 1. Modeled wireless link behavior for a single-element WiGig transceiver for various PHY data-rates. Blue triangle symbols are for measured LOS results for [3], and square symbols in orange are for this work. With the exception of the highest data -rate result, which is slightly worse than predicted, the model accurately predicts the realized system performance.

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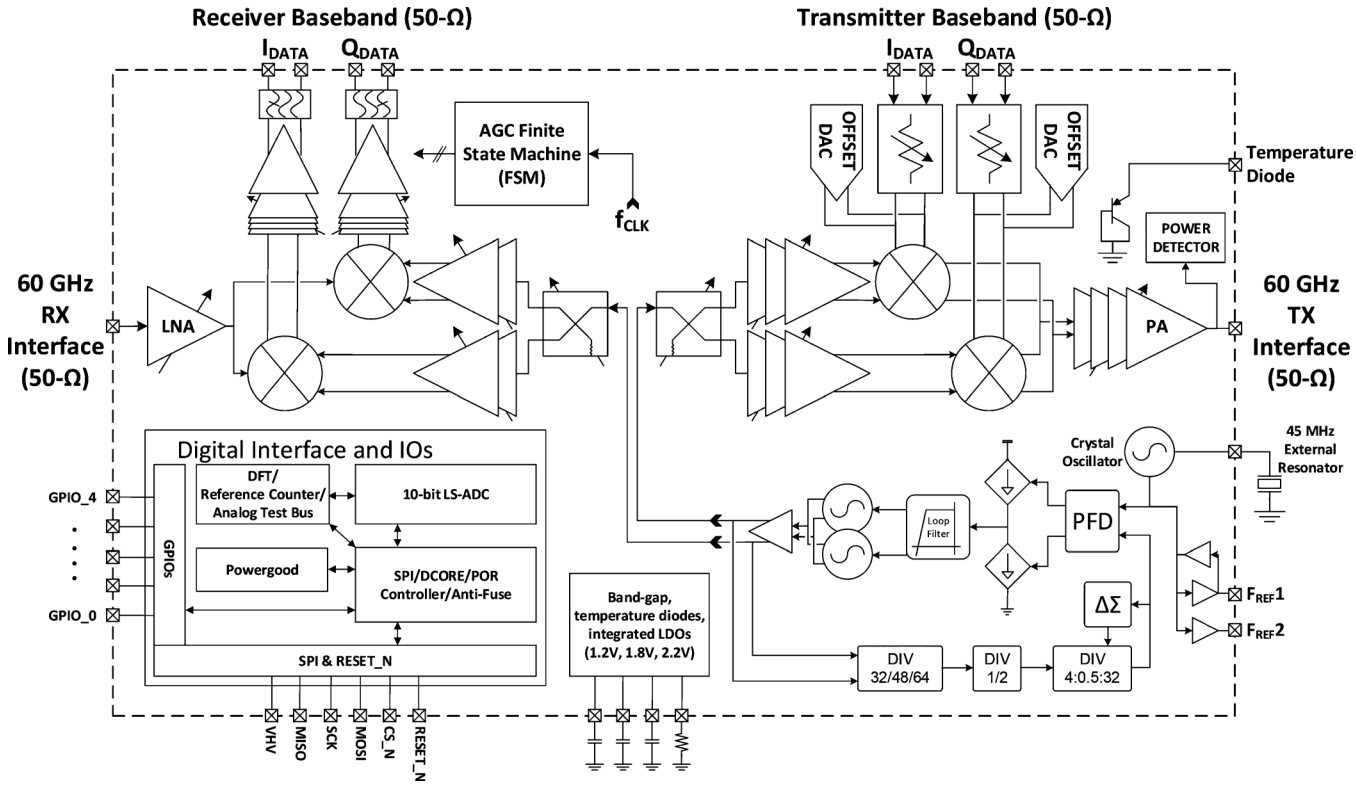

Fig. 2. Block diagram of the transceiver.

This paper presents a fully integrated, 802.11ad-2012/WiGig compliant transceiver that utilizes high-performance 130 nm SiGe:C BiCMOS technology in conjunction with an optimized direct-conversion architecture resulting in very high link-performance without the use of a phased-array [18]. The use of high output power and low noise figure SiGe BiCMOS technology, combined with specific architectural and design choices results in a maximum level of performance for a given area and power-consumption budget.

This paper is organized as follows. Section II presents results from a model of the expected performance of a WiGig transceiver, and Section III describes the transceiver design and implementation in detail. Section IV shows measurement results at a block level, and Section V shows measurement results at the system and standards level. Finally, a performance comparison is carried out in Section VI, followed by a summary of the paper in Section VII.

II. WiGig Performance Modeling

System models have been developed to guide the 802.11ad/WiGig transceiver design choices. Using standard channel propagation models, IC-specific performance metrics and known sensitivities for various modulation and coding schemes, link distance estimations can be calculated for various data-rates. The result is shown below, and more detail is given in the Appendix.

The data-rates shown in Fig. 1 are the effective 802.11ad/WiGig physical layer (PHY) data-rates, which include the low-density parity-check (LDPC) error-correction coding overhead but excludes the impact of any higher level protocol. The sensitivity is defined at a 1% packet-error rate (PER). For the antenna-integrated packaged solution, results are shown for both a line-of-sight (LOS) model and a none-line-of-sight model (NLOS), which consists of a two-reflection path. Results are shown for both the current generation silicon represented by this work, and a previous design [3]. Measured results, which will be fully described in Section V, follow the trend of the model's predictions, except for the highest data-rate point, where the measured results are slightly worse than expected. At this top data-rate, the performance limitations deviate from mainly thermal contributions to other impairments like non-linearities of the transmitter and phase noise of the local oscillators.

III. Transceiver Description

Designed using a 130 nm SiGe:C BiCMOS technology [19], the transceiver, shown in Fig. 2, implements direct-conversion transmit and receive architectures with a fundamental-frequency PLL and integrated crystal oscillator. The design of these major blocks will be described in the following sub-sections along with a selection of sub-blocks that provide testability and configuration options. Certain components of the implemented system have previously been presented [3], [18], and this will be indicated when appropriate.

A. Transmitter

The transmitter is a direct-conversion design that supports differential I/Q zero-IF inputs and a single-ended 60 GHz output. Variable gain is implemented in the baseband and RF sections through switched baseband attenuators and

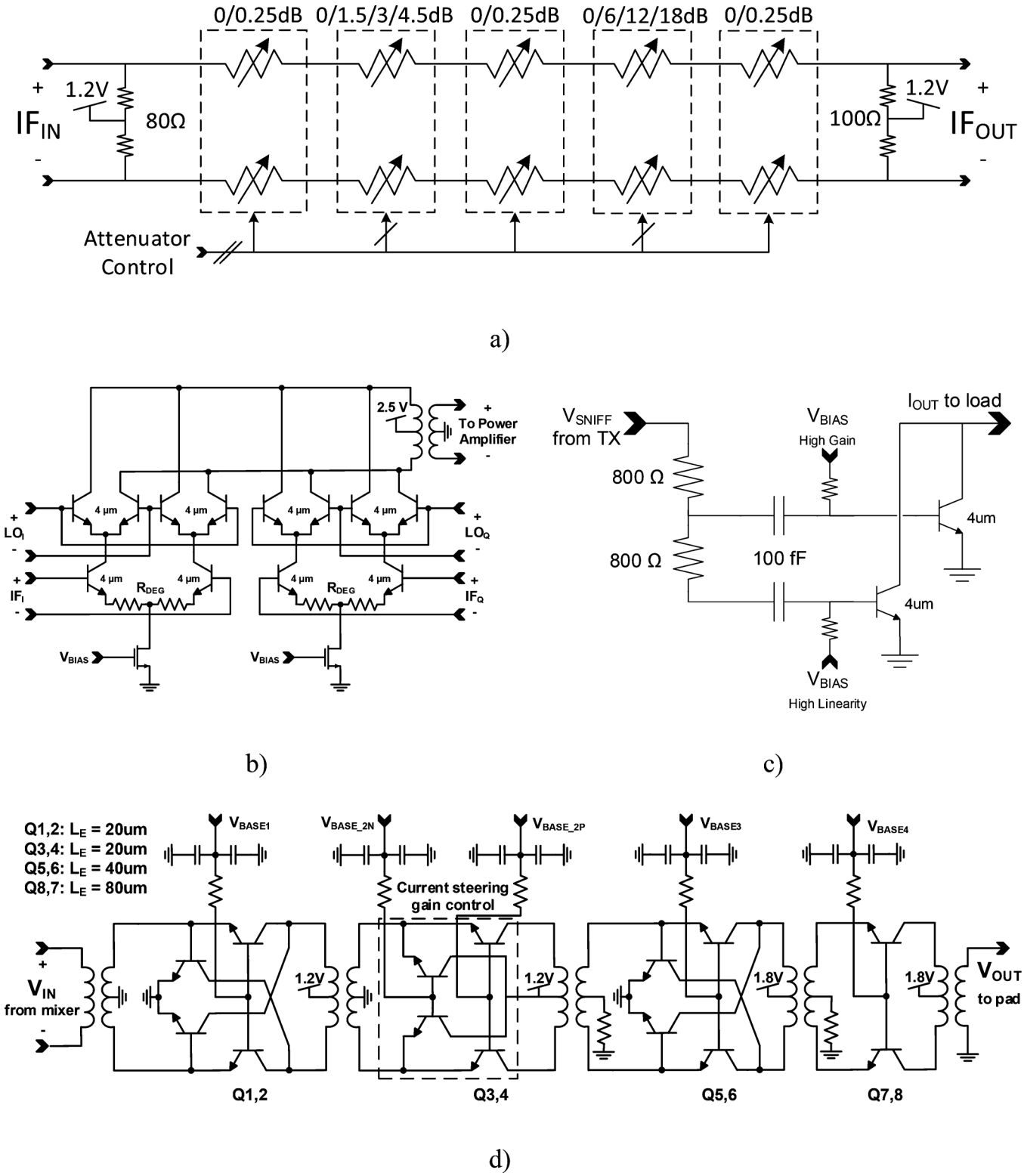

Fig. 3. Key transmitter building block schematics, including: (a) baseband stepped attenuator, (b) transmit up-convert mixer, (c) dual-range RF power detector, and (d) the output power amplifier.

variable-gain RF amplifiers. DC-offset DACs are integrated for LO leakage suppression. Phase/amplitude control is available in the LO distribution path for image rejection correction and calibration. Multiple integrated power sensors are included as well as a temperature sensing diode with a dedicated output pad.

1) Baseband Stepped Attenuator: The baseband input path of the transmitter has been designed to achieve high linearity and low noise across a wide range of input signals levels using programmable attenuators. Shown in Fig. 3(a), the programmable attenuator consists of a passive (resistive) stepped-attenuator,

implemented using a series of cascaded π- and bridged-T sections, each with programmable switched resistances to achieve an attenuation range of 23 dB with steps of 0.75 dB. The 0.75 dB LSB is implemented using individual 0.25 dB cells that help ensure uniform step size.

2) Up-Convert Mixer and LO Buffers: The transmitter LO path takes a single input from the PLL, generates quadrature signals, and buffers them to drive the transmit up-convert mixer. The mixer performs direct up-conversion of the I and Q baseband signal and combines them at the output to drive the PA with a modulated 60 GHz signal. The quadrature LO signals are generated using a lumped 90° hybrid [20], [21] with added phase-tuning to support quadrature phase correction/calibration. The I and Q paths of the LO buffer have independent variable gain and bias control to support amplitude offset correction/calibration. The mixer includes an integrated power sensor on the LO inputs to support this amplitude offset calibration.

The mixer, shown in Fig. 3(b), is a double-balanced Gilbert cell that operates from a 2.5 V supply and uses resistive degeneration for reduced gain and improved linearity. The I and Q signals are combined at RF in the load transformer, which also acts as the input to the power amplifier. Not shown in the schematic is a series of adjustable "bleed currents" [22], situated at the collectors of the transconductor HBTs, which can provide a tradeoff between linearity and noise figure performance.

3) Dual-Range RF Power Detector: The output power of the power amplifier is resistively sensed using a dual-path power detector, shown in Fig. 3(c). Two paths are provided (only one of which is active at a time), a high-gain path for low-power leakage signal level detection, and a high-linearity path for output signal level calibration. The two detector HBTs drive a common programmable load resistor, followed by programmable post-amplifiers with selectable 0/24/48 dB voltage gain (with offset correction). A reference HBT device is available for normalizing the detected voltage to a zero-reference. In high-linearity mode, the detector has a sensitivity of between 10–12 mV/mW, and in high-gain mode, the sensitivity is around 60 mV/mW. The high-linearity sensitivity value results in the detector output voltage remaining below 500 mV up to around 16 dBm.

4) Output Power Amplifier: The schematic of the power amplifier is shown in Fig. 3(d) with emitter lengths (L_E) indicated for bipolar devices Q1–8. It is a 4-stage common-base, transformer-coupled design. Stages 1 and 3 utilize capacitive-neutralization feedback [23] to boost the gain with cold-biased HBTs cross-connected between emitters and collectors. Stage 2 implements RF-path gain-control using current steering to either the signal path or AC-ground. Stage 4 drives off-chip using an output transformer to convert from differential to single-ended. The secondary coil of the transformer also enables ESD protection by providing a low-impedance ground connection at frequencies relevant to ESD events [24], thus protecting any devices at the PA output. In order to optimize the broad frequency response of the amplifier, the resonance frequency for each stage was slightly staggered, with stage 1 and stage 2 centered slightly lower in frequency (57–58 GHz), stage 3 centered higher in frequency (65 GHz), and stage 4 centered around the middle of the band (60 GHz). The PA is designed to provide output compression points beyond +13.5 dBm over the whole 60 GHz frequency band (57–66 GHz).

B. Receiver

The receiver is a direct-conversion design like the transmitter that supports differential I/Q zero-IF outputs and a single-ended 60 GHz input. The RF portion of the receiver is partially based upon [3], but the general description will be repeated here for convenience, and differences will be indicated. The receiver baseband VGA and automatic gain-control (AGC) is new to this work.

1) Low-Noise Amplifier: The low-noise amplifier, with no major changes from [3], is a 3-stage design with an output common-base stage that implements variable-gain control. The input stage is noise-matched to 50 Ω in the presence of the expected bump-pad capacitance and offers a low-impedance DC path to ground for ESD protection.

2) Down-Convert Mixer and LO Buffers: The I/Q LO generation for the receiver is similar to the transmitter side. A lumped-element, transformer-based quadrature hybrid is used to generate I/Q signals from a single input signal from the PLL. Active buffers are used both to amplify and to generate differential signals for the mixer. This design revision adds quadrature phase (in the hybrid) and amplitude (in the amplifiers) offset adjustment/compensation capabilities. The design has also been enhanced from [3] for robust frequency and gain coverage through optimizing passives and improving power and ground distribution networks.

The down-convert mixer contains only minor re-tuning compared with [3] for improved inter-stage matching, signal distribution, and floor-planning. It utilizes in-phase active power-splitting to generate I and Q signals, and couples the signals from the two transconductor HBTs into the mixing-quad using a transformer. This transformer permits: 1) the generation of differential input signals for the double-balanced Gilbert cell mixing quad, and 2) an AC current-folding that relaxes the headroom requirements of this design from a traditional "stacked" double-balanced active mixer design. Robust operation of a traditional stacked HBT-based design from a single 1.8 V supply would not be possible.

3) Baseband Variable Gain Amplifier: Constructed from a cascade of four variable gain stages and a fixed-gain 50 Ω output driver, the baseband VGA is designed to provide uniform sub-1 dB gain steps over almost 50 dB dynamic range while providing approximately 1 GHz bandwidth. Fig. 4(a) shows the distribution of digital variable-gain control in the VGA (as well as the whole receiver), along with the positions of various peak-detectors and their associated comparators that are used to monitor signal levels during operation and to provide feedback to the AGC state machine.

Each variable-gain stage provides approximately 12 dB of gain-control range which is implemented using a differential HBT amplifier cell with programmable emitter degeneration. Emitter degeneration is controlled using a bank of switched resistors placed across the differential node. Along with the VGA cell's schematic shown in Fig. 4(b), the schematic for the 50 Ω output driver, an emitter-follower buffer operating from 1.2 V,

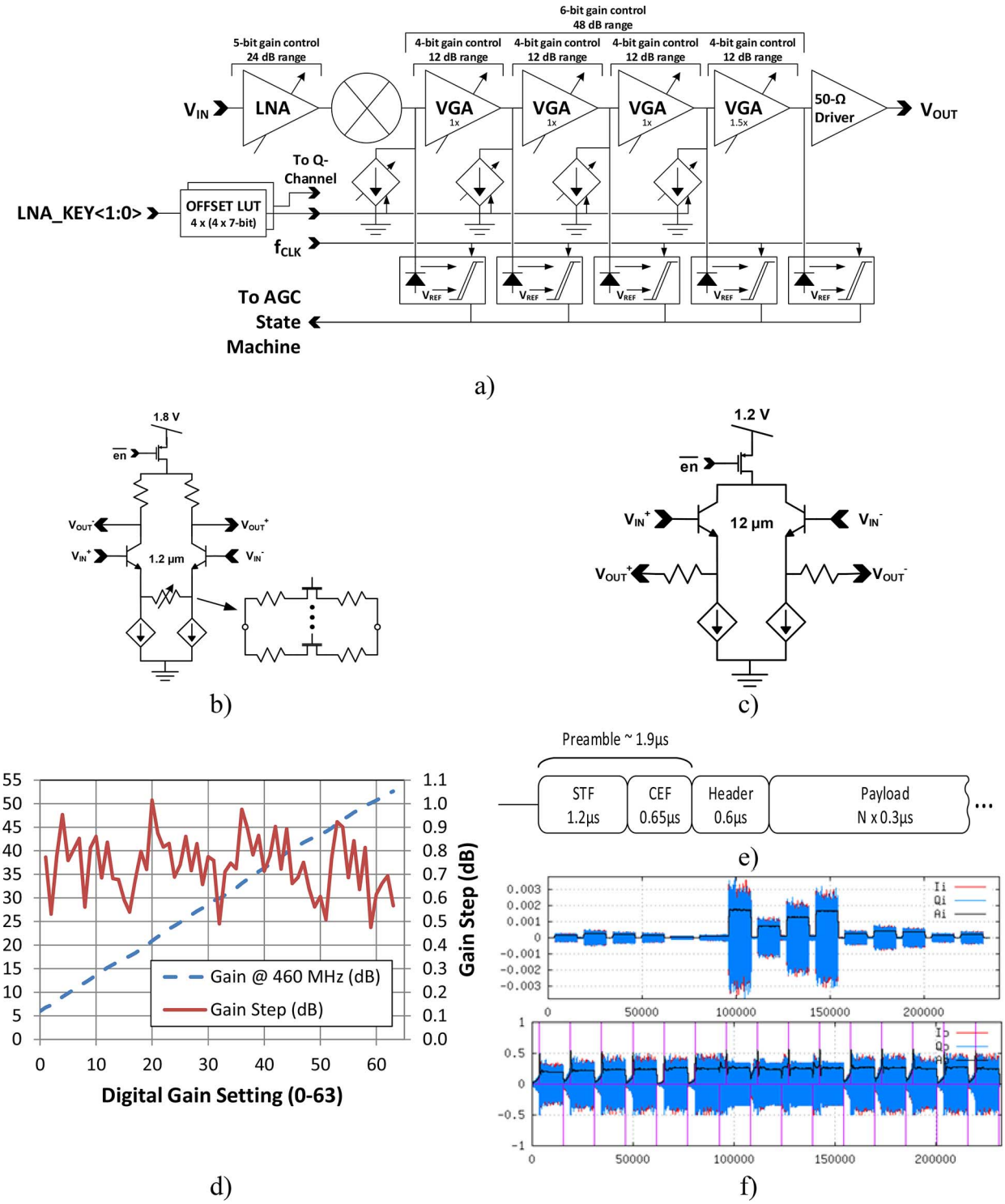

Fig. 4. (a) Block diagram showing the distribution of various digital gain-controls within the receiver between different stages at both RF and baseband. Also shown are the positions of the various peak detectors, comparators, and offset compensations DACs. The schematics for the 1× VGA stage, (b), and the 50 Ω output driver, (c), are also shown. Measured gain and gain-step are shown in (d). The packet structure for the WiGig standard is shown in figure (e) and the simulated AGC convergence for various WiGig test-packets is shown in (f) for various input packets (top) and the resultant output (bottom).

can be found in Fig. 4(c). To ensure stable operation without oscillation, a fully differential topology was used with extensive power-supply decoupling and careful bias-network design with appropriate isolation. A measurement of the baseband VGA's performance is provided in Fig. 4(d) (from a stand-alone test-structure) showing just under 50 dB dynamic range, from 6 to 53 dB, and a gain-step that is between 0.5 and 1 dB for all adjacent settings.

Also shown in Fig. 4(a) are the four offset compensation DACs present on both the I- and Q-baseband paths that are used in the integrated digital feed-forward DC-offset cancellation system, critical for high-gain and/or DC-coupled homodyne

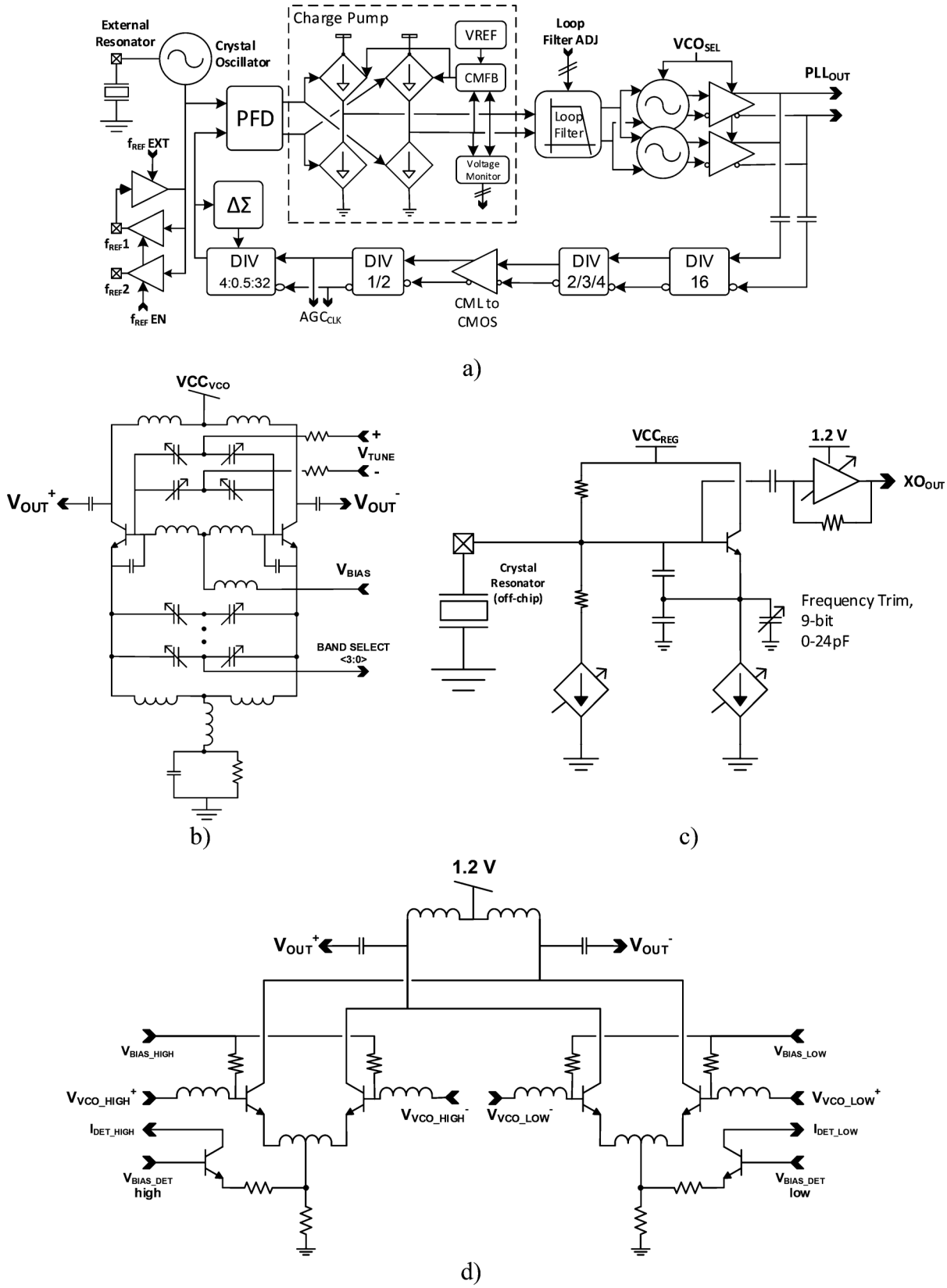

Fig. 5. The block diagram of the dual-VCO PLL in (a) along with the schematics of some key blocks including (b) the VCO, (c) the crystal oscillator (XO), and (d) the VCO selector buffer.

direct-conversion systems. An integrated calibration process configures the four 7 bit DACs to eliminate both static (mismatch related) and dynamic (self-mixing related) offsets from the baseband receive path to a target of below 1 mV at the output of the receiver. To accommodate potentially varying LNA RF-path gain, the calibration routine pre-determines up to

four separate sets of calibration settings which are automatically selected by the AGC state-machine during gain convergence.

4) Receive Automatic Gain Control: The 802.11ad/WiGig protocol requires that the receiver be capable of receiving packets with a wide dynamic range of powers, approximately -78 to -33 dBm, at any given time (with no specific or presumed correlation between the powers of adjacent packets). Additionally, due to the packet structure as shown at the top of Fig. 4(e), the receiver AGC must be settled within 1.2 μs of the packet start in order to correctly receive the channel estimation field (CEF), which is critical for the baseband modem to operate. The STF (short training field) period of the preamble offers repeating signal patterns (Golay complementary sequences) that can be used to drive, among other things, the symbol-rate recovery block in the baseband, as well as AGC functionality in the receiver.

To achieve the required wide-dynamic range of operation and rapid convergence, the AGC implements a multi-stage variable gain architecture with parallel power sensing feedback. The variable gain is implemented digitally with fine control at baseband, with <1 dB gain-step size, and more coarsely at RF within the LNA, with larger programmable step sizes and about 24 dB of additional dynamic range. The gain-convergence is performed in two steps: 1) a rapid convergence to within 6 dB over approximately the first 300 ns, followed by 2) a progressive convergence to within 1 gain-step (± 0.8 dB) of the final target over the next 1 μs, before the start of the CEF. The two plots in Fig. 4(f) show the results of a mixed-signal simulation of the receiver AGC operating with input packets of a wide range of modulation schemes and input powers (SNRs) over time, in ns (top), and the corresponding outputs (bottom) from the receiver, showing well controlled average output levels. The levels for the bottom figure are aligned with the full-scale of the baseband ADC, here normalized to ± 1.

C. PLL With Dual-Bank VCO

Frequency generation for the transceiver is provided by a fundamental frequency PLL that is based upon the frequency synthesizer from [3], but has had a number of optimizations and improvements made with the goal of improved frequency coverage and phase-noise performance. The PLL covers the four standard 802.11ad/WiGig channel center frequencies while operating in integer mode (58.32, 60.48, 62.64, and 64.80 GHz), and additionally offers half-channel steps when using the 0.5-integer divider. Additionally a delta-sigma modulator can be enabled to provide fine-grained frequency selection ($<$1PPM) with a penalty in integrated-jitter performance.

1) Dual VCO-Bank With Integrated Selector and Power Detectors: To ensure robust frequency coverage of the entire world-wide 60 GHz frequency band (57–66 GHz), a dual VCO-bank design has been implemented to ease the tuning-range requirements of the individual oscillators. A common topology has been implemented for both high- and low-band VCOs, as shown in Fig. 5(b), with specific tank and load inductor designs for the high and low frequency VCOs. The core design utilizes a modified Colpitts topology [25] with the placement of fine-tuning varactors in the base/tank node in addition to the traditional varactors in the emitter, which are used for coarse band selection. In this design, 4 bit coarse-band selection in conjunction with high/low-band VCO selection provides 32 tuning band options for the 9 GHz frequency range.

Dynamic selection between the two VCOs is achieved using (in addition to VCO-specific biasing control) a combined VCO buffer/selector circuit shown in Fig. 5(d), which provides both isolation as well as signal-level amplification. Additionally, the buffer offers a simple VCO power indicator by sensing small changes in the voltage across the emitter degeneration resistor. This VCO power monitor signal is used as part of a robust VCO calibration scheme which optimizes fine-tune varactor voltages in conjunction with VCO and VCO-buffer/selector biasing conditions.

2) Integrated Crystal Oscillator With External Resonator: The crystal oscillator circuit, shown in Fig. 5(c), has been optimized to improve its negative resistance generation (and thus its startup margin) as well as the tuning range in order to better tolerate a wide range of operating conditions and variation. The HBT-based oscillator core is designed to generate in excess of 1.5 kΩ of negative resistance, and simulations confirm that at least 400 Ω of negative resistance is presented to the crystal resonator at the chip-interface for all targeted operating conditions (including all loading circuitry, biasing, ESD diodes, and expected stray capacitances). This is sufficient margin to enable operation with cost-effective or very small foot-print crystal resonators which typically have modest to high equivalent series resistance (ESR) parameters and are popular in consumer electronics or mobile applications. This design expects ESRs in excess of 100 Ω. Additionally, a large digitally controlled capacitor array with an LSB step $<$50 fF and a total range up to 24 pF is available for fine-frequency adjustment to compensate for frequency-drift during operation or static offsets between parts. Frequency resolution below 0.5 PPM is achievable even with a wide tuning range of about 70 PPM.

Finally, signal levels in the tank and output buffer/level-shifter design have been improved to ensure a reduced phase noise floor over all conditions and consequently a reduced jitter contribution from the reference oscillator to the overall PLL operation. The phase-noise for the crystal oscillator has a noise floor below -165 dBc/Hz from a 30 kHz offset and above.

D. Transceiver Biasing, Support, and Control Circuitry

An integrated band-gap with fine-voltage trimming and multiple LDOs provide stable and robust biasing and power supplies. Multiple programmable GPIOs and a 4-wire SPI interface ensure fast and robust control over all operational features. The GPIOs also permit the rapid selection of various chip operating states, including receive/transmit operating selection and fine control of the receiver AGC operation.

Numerous features are included on the chip for robust and effective testing and configuration of the transceiver. A low-speed sensing ADC (LS-ADC) has been included that offers 10 bit resolution with an INL less than 0.5 LSB (after one-time calibration) and a 1 MHz sample rate. A high-precision reference counter provides the ability to either frequency tune the integrated crystal oscillator to less than 1 PPM (using an external high stability reference clock) or to monitor any internal clock signals including the 60 GHz VCOs or the bank of process-

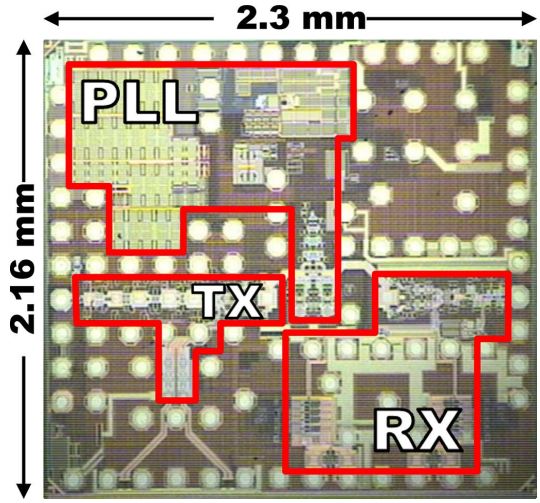

Fig. 6. Die micrograph of the transceiver showing the 2.3×2.16 mm^2 $=$ 4.97 mm^2 dimensions.

tracking ring-oscillators. For process tracking, in addition to the ring-oscillators, resistor sheet resistance and contact/via resistance can be monitored using calibrated reference voltages and currents.

Analog test and sensing signals from throughout the chip (such as power-detector outputs or LDO voltage read-back) are routed and multiplexed to common test-points where they can be either internally monitored using the LS-ADC, or multiplexed on to any of the GPIO pins for external measurement.

A dedicated pin is offered with a direct connection to a standard PN-junction thermal diode (located in close proximity to the transmitter power amplifier) that can be monitored externally using industry-standard sensors. Alternatively, the diode can be monitored using internal temperature sensing circuits with $\pm 5^{\circ}$C accuracy. For the internal monitoring option, additional thermal diodes are available in the PLL and the process tracking block.

Finally, a range of factory-level calibration data is stored on-chip in a bank of one-time programmable anti-fuse cells that includes LS-ADC calibration, band-gap trimming, and crystal-oscillator frequency normalization.

IV. Block Performance

A. Manufactured IC and Packaging

A die micrograph of the manufactured transceiver IC is shown in Fig. 6 with a total area of 2.3×2.16 mm^2 $=$ 4.97 mm^2. The design utilizes flip-chip bumps with 160 μm pitch organized in a non-uniform array. From 1.2, 1.8, and 2.5 V supplies, the chip consumes 340 and 720 mW in receive-mode and transmit-mode, respectively. Under relaxed phase-noise requirement conditions, a further 50–60 mW of power can be eliminated through reduced biasing in the VCO and charge-pump circuits.

Two different packaging/interface solutions are presented in Fig. 7. First, in Fig. 7(a), is a high-performance ceramic-substrate version, where the IC is mounted directly along with key passive components and offers an industry-standard WR-15

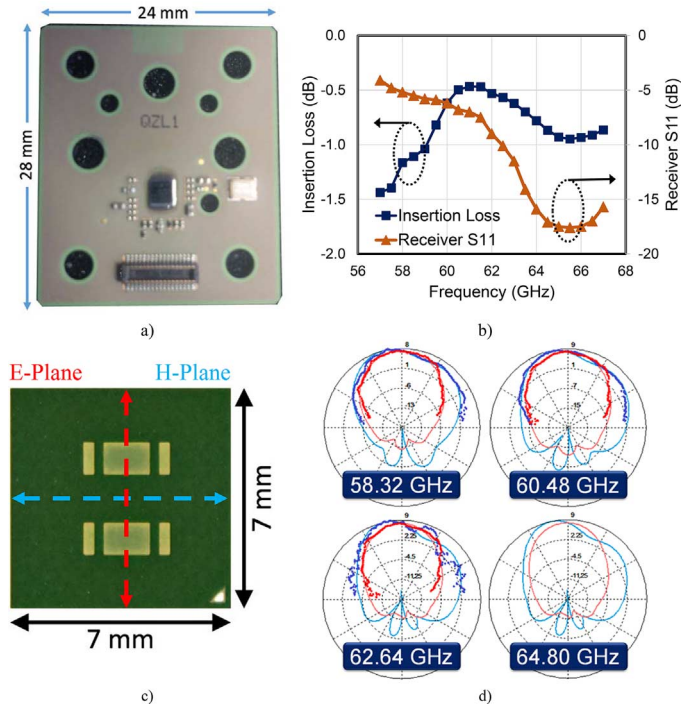

Fig. 7. Transceiver packaging options: Substrate-integrated wave-guide transition module (a) and the measured insertion and return loss (b), and the antenna-integrated package (c) with radiation patterns (d). The E- and H-plane radiation patterns are shown in red and blue, respectively.

waveguide interface. The 24×28 mm^2 substrate includes a 45 MHz crystal resonator and a low-profile 30-pin connector that is used for all IC-related signals (low-frequency control as well as baseband I/Q signals) and power supplies. The substrate includes the necessary mounting holes to directly attach to a waveguide flange. A compact, low-loss, wide-band and low-cost transition to waveguide has been designed and optimized in the presence of the flip chip bump and the die. The same transition has been used for dedicated transmit and receive versions of the module (utilizing the same IC). The transition performance, as shown in Fig. 7(b), shows an insertion loss below 1 dB for most of the 60 GHz band and a return loss better than 5 dB across the band, and better than 10 dB from 62 to $>$67 GHz. The transition has been characterized by measuring a back-to-back test structure, which is a waveguide to CPW transition followed by a 2 cm 50 Ω CPW line followed by an identical CPW to waveguide transition. To de-embed the CPW line effect, three CPW lines with different lengths have been fabricated on the same substrate and measured with on-wafer GSG probes. These waveguide-interface modules were used for the majority of system characterization and the insertion loss of the transition was de-embedded for all transmit-related results but not for the receiver results.

In addition to the wave-guide modules, an antenna-integrated package was implemented in a low-cost organic material. Shown in Fig. 7(c), the package is 7×7 mm^2, utilizes a 0.5-mm-pitch BGA, and is less than 0.8 mm thick when fully mounted on standard PCB. Dedicated receive and transmit antennas are integrated, and offer approximately 8 dBi gain (Fig. 7(d)) across the four 802.11ad/WiGig channels.

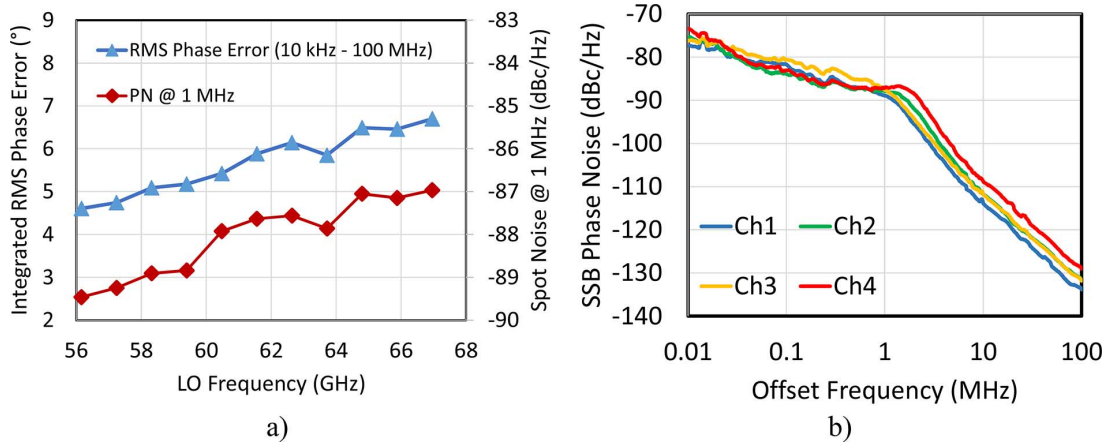

Fig. 8. (a) PLL RMS phase error (integrate from 10 kHz to 100 MHz) and spot frequency (@ 1 MHz) vs. LO center frequency. (b) PLL phase-noise curve for difference channel frequencies.

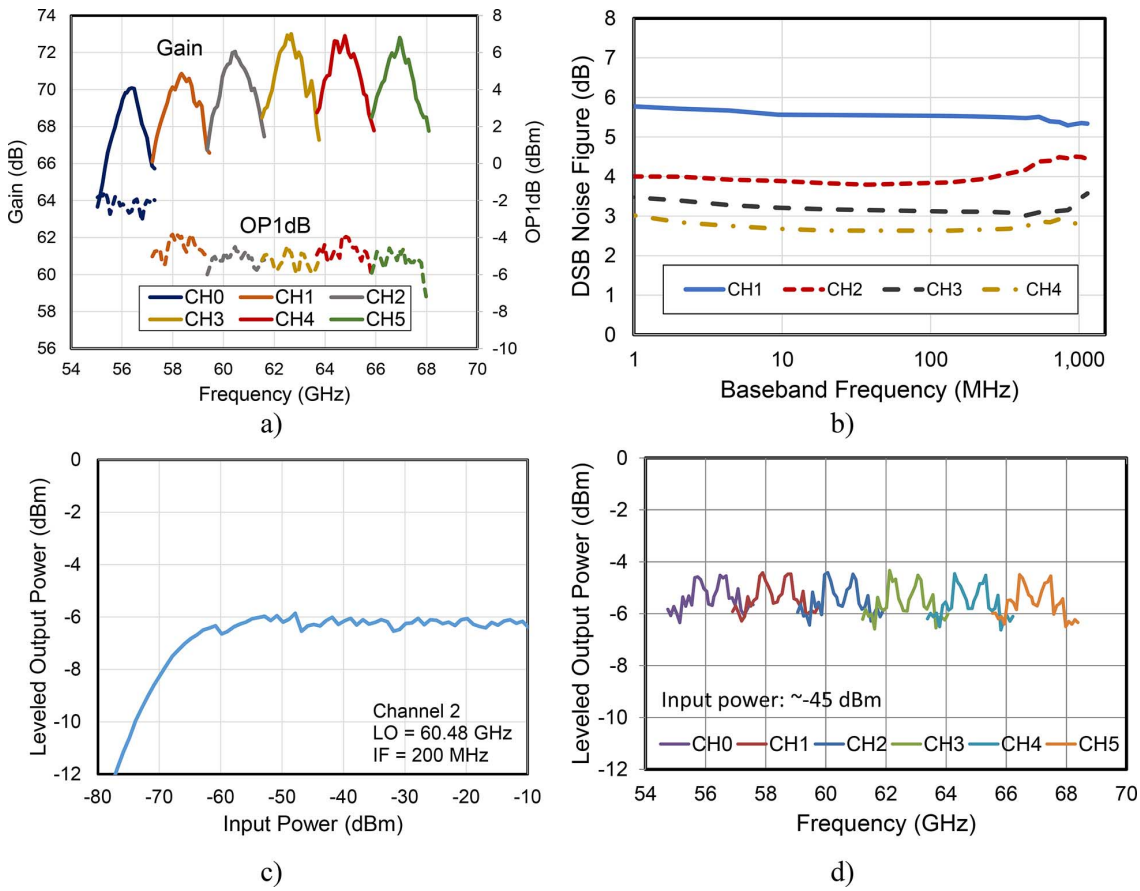

Fig. 9. Receiver performance results: conversion gain and OP_{1db} for fixed LO frequencies and swept RF around the channel centers (a) and DSB NF versus baseband frequency (b). Receiver AGC output leveling vs. input power (c) and receiver AGC output leveling for various LO center frequencies with swept RF input tones (d).

B. PLL

The integrated PLL covers the 60 GHz frequency band with margin, extending over 1 GHz below and above the standard frequency band edges (57 and 66 GHz). Fig. 8(a) shows the PLL integrated phase-noise (in degrees-RMS) for the closest available integer or 0.5x-integer center frequencies. Additionally, the VCO spot-noise at 1 MHz offset is shown. The phase-noise results for the four standard 802.11ad/WiGig channel frequencies are presented in Fig. 8(b) where the nominal loop-bandwidth for the PLL is around 2 MHz.

C. Receiver

The receiver provides a flat frequency response across more than 10 GHz of center-frequency settings. The plot in Fig. 9(a) shows approximately 3 dB of variation at maximum gain across ±900 MHz around the channel centers, and has a

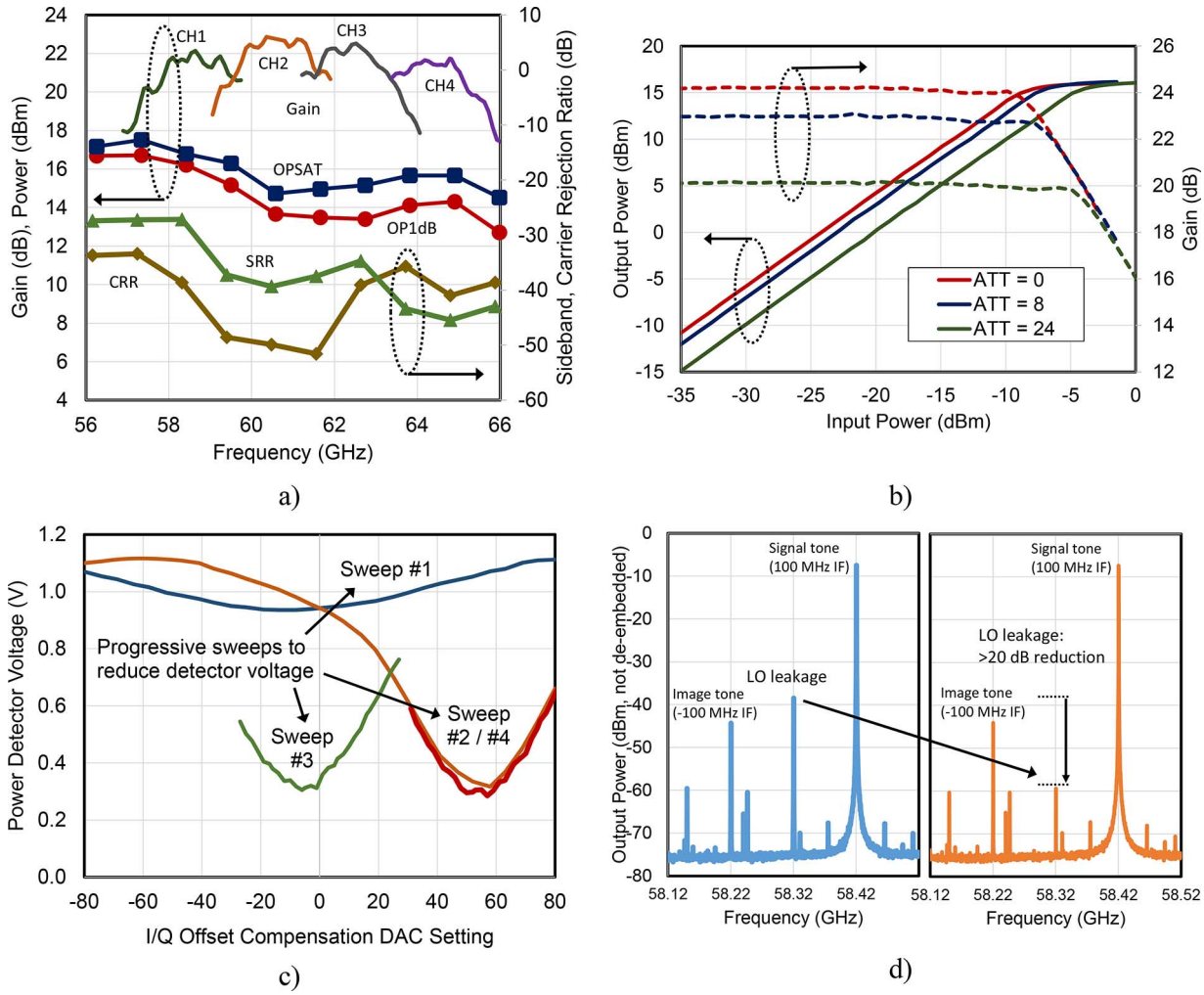

Fig. 10. (a) Transmitter gain, OP_{1dB}, and P_{SAT}, sideband and carrier rejection ratio (CRR, SRR) for swept LO frequency (with constant IF). Additionally, gain curves are shown for channel 1–4 with swept IF frequencies. (b) Swept power/gain curves for channel 1 with three different baseband digital stepped-attenuator settings. The OP_{1dB} for the shown settings is constant at +15.6 dBm. Example of LO leakage calibration (c), with the resulting impact on the output spectrum (d).

stable output compression points of between −5 to −4 dBm. Flat baseband frequency response is available with less than 1 dB of noise-figure variation observed within each channel in Fig. 9(b). The degraded noise-figure result in channel 1 is a consequence of the waveguide transition mismatch at the receiver input in the frequency range below 61 GHz.

The robust operation of the receive AGC is demonstrated in Fig. 9(c) and (d), where the first figure shows AGC's output leveling ability against a swept input signal from −80 dBm up to −10 dBm. From −70 dBm, the output signal is kept with 2 dB of the target output level of −6 dBm. When the center frequency and baseband frequency is varied, the receive AGC is able to offer consistent and stable output powers, as shown in Fig. 9(d).

D. Transmitter

The transmitter output 1 dB compression and saturated power frequency response is shown in Fig. 10(a) for a constant baseband input frequency, and a swept LO frequency. The output 1 dB compression and saturated power reach 16.5 dBm and 17.5 dBm, respectively, and vary by less than 3 dB over the frequency band between 57 GHz and 66 GHz. The gain is shown for fixed LO frequencies (equivalent to the 4 WiGig channels), with swept IF around channel centers, showing gains between 22 and 23 dB and −3 dB responses greater than ±1 GHz. Additionally, the sideband and carrier rejection ratio (SRR and CRR, respectively) are shown for swept LO frequency. The CRR is shown after performing leakage calibration (described below). The SRR is better than −25 dB across the band, and better than −30 dB for frequencies above 59 GHz. The CRR is better than −35 dB for frequencies above 58 GHz. The functionality of the stepped-attenuator is demonstrated in Fig. 10(b), where three digital attenuator settings are selected, the input power is swept and the corresponding output power and gain is recorded. Across the range of attenuator settings, the output P_{1dB} remains constant at +15.6 dBm, while the input P_{1dB} improves with the added attenuation.

An example of standard LO leakage suppression calibration is shown in Fig. 10(c) and (d). The 9 bit resolution (8 bit plus sign) current-DACs are swept to generate small DC offsets at the I and Q baseband inputs, and the corresponding LO leakage

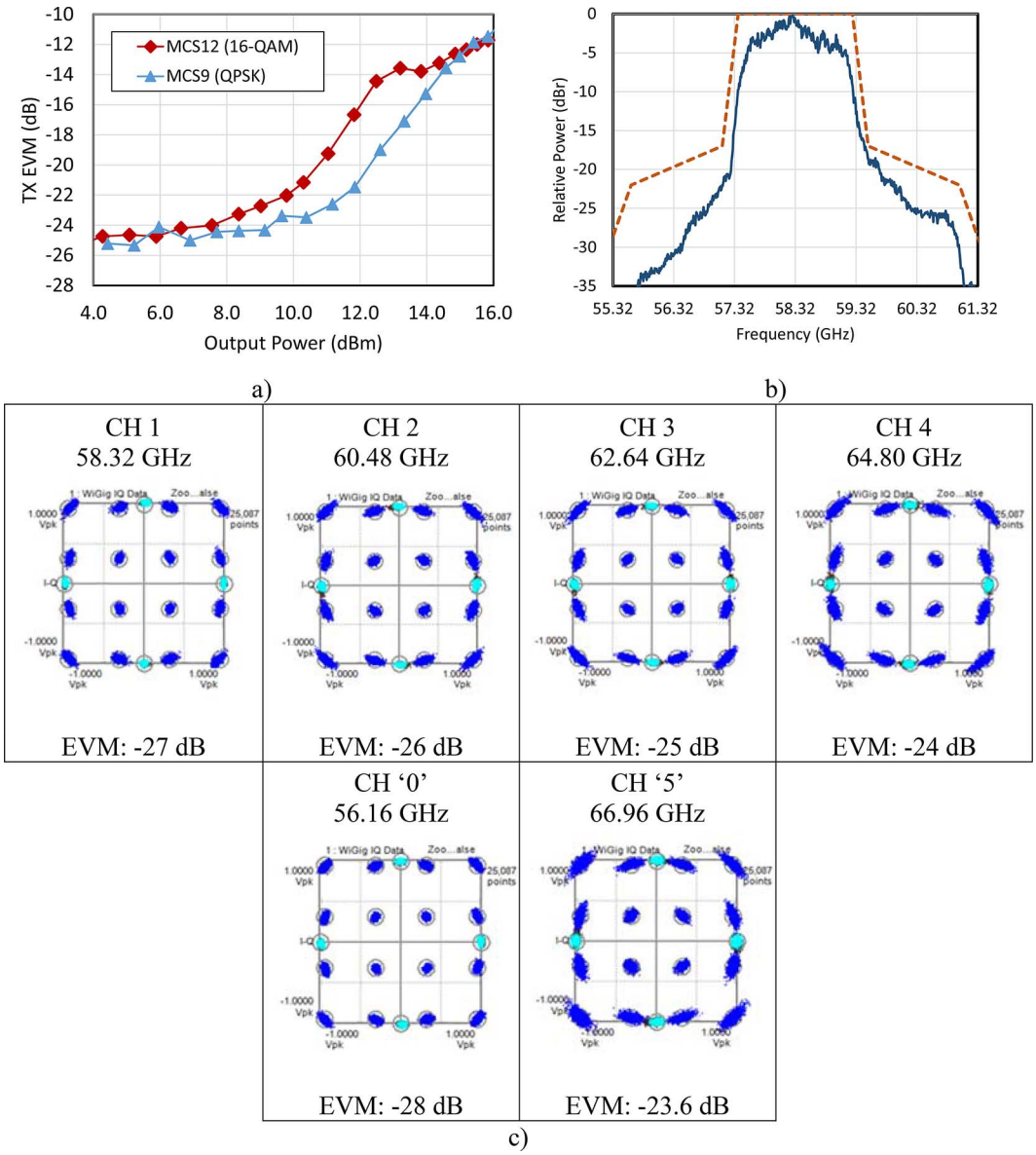

Fig. 11. Measured transmit EVM vs. TX output power for channel 1 (58.32 GHz) (a), and the transmit mask for MCS9 operation at +14 dBm (c). MCS9 EVM compliance (−15 dB) is met up to 14.1 dBm, and MCS12 compliance (−21 dB) is met up to +10.4 dBm. Additionally, (c) shows the measured peak transmit EVMs (at ∼ 5 dB back-off) for all 802.11ad/WiGig channel centers, including non-standard channels '0' and '5'.

signal is measured at the PA output using the RF power detector. Rapid convergence is achieved by using sequential sweeps on the I and Q paths before a final sweep on the I path results in an optimized leakage level. An additional sweep is shown for the Q path where no further reduction in the detected leakage is observed. The final output leakage level is limited by the sensitivity of the RF power detector in high-gain mode, and not by the offset DAC resolution. The calibration typically reduces the LO leakage by more than 20 dB, to levels below −35 dBc, which is sufficient to mitigate any potential degradation of overall signal fidelity.

V. System Level and Link Testing

A. Transmit EVM and Output Power

Transmitter and full link (TX-RX) characterization was carried out using 802.11ad/WiGig compliant packets generated by a waveform generator being fed data from a software package (Keysight 81199A Wideband Waveform Center) that implements a standard-compliant baseband and can both generate and analyze WiGig packets. For transmit EVM testing, a test-fixture was used that utilizes the wave-guide packaged IC in conjunction with a reference receiver built from off-the-shelf waveguide components (Quinstar WR-15 mixer) and laboratory signal generators (Agilent E8257D). The down-converted signal is then captured/digitized using a broadband Agilent oscilloscope and then analyzed using the 81199A WWC software.

Fig. 11(a) shows the measured transmit EVM for a range of output powers for both MCS9 (QPSK data with a 2.502 Gbps effective PHY data-rate) and MCS12 (16-QAM data with a 4.62 Gbps effective PHY data-rate) signals. Here, the output power was measured separately from the EVM using a waveguide power sensor connected directly to the test module. The 802.11ad standard requires worst-case EVMs for MCS9

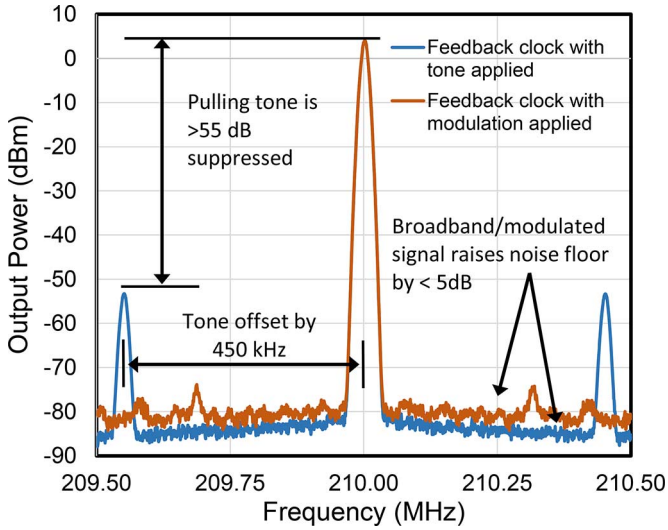

Fig. 12. An example of VCO pulling by high-power transmitter operation. Single-tone operation (blue trace) at ∼14 dBm output power results in a −55 dB spur in the PLL divider path (divide-by-288). High-power WiGig packets (red trace), >13 dBm, result in a minor, <5 dB increase in the observed noise floor.

at −15 dB and MCS12 at −21 dB. The results show standard compliant EVMs for MCS9 at 14.1 dBm and MCS12 at 10.4 dBm. For the MCS9 case, the corresponding output transmit mask is shown in Fig. 11(b) for an output power of +14 dBm. The best-case EVMs for all channel centers while operating at MCS12 are shown in Fig. 11(c), where the EVM was measured at back-off. Channels 1–4 show at least 3 dB margin from the required −21 dB EVM. Results for non-standard channels '0' and '5' (56.16 and 66.96 GHz) are shown in order to demonstrate the wide frequency coverage of the system.

A design concern when implementing a direct-conversion architecture with a fundamental frequency VCO is the possibility of VCO-pulling by the power amplifier [26]. The transmit EVM testing does not indicate any specific issues relating to this consideration for this work, but the presence of VCO-pulling can be confirmed by looking at the PLL feedback divider signal in the presence of a high-power low-IF tone at the transmitter output. Fig. 12 shows the results when looking at the divider output with a 450 kHz signal being applied and a resultant output power of around +14 dBm. Spurs can be seen in the spectrum around the 210 MHz carrier (60.48 GHz ÷ 288) offset by 450 kHz with powers 55 dB below the carrier. Under normal operation with a high-power modulated signal applied to the transmitter (generating >13 dBm at the output), only a small, less than 5 dB increase in the noise floor is observed. These observations, along with the robust transmitter EVM testing results, indicate that VCO-pulling is not a significant factor for a broad bandwidth system like this work, where only a small fraction of the signal power lies within the pulling bandwidth of the VCO.

B. Full Link Testing and Receiver Sensitivity

Full link (TX-RX) performance was tested using setup as shown in Fig. 13(a), where the lab equipment and off-the-shelf down-converter have been replaced by a receiver test-module. Additionally, a set of fixed and variable attenuators are placed in the waveguide path in order to facilitate a wide-range of signal levels. An example of a full-link EVM is shown in Fig. 13(b) for a high SNR condition where an EVM of −22 dB is achieved in channel 1.

By controlling the level of attenuation between the transmitter and receiver test-modules, the receiver sensitivity was examined. Fig. 13(c) shows the measured receiver sensitivity across the whole range of MCS levels (here shown by their corresponding data-rates on the x-axis) with the top-trace showing the standard specification for minimum sensitivity. For these results, the sensitivity level was determined for all channel center frequencies (from 1–4), and the worst value used. These results demonstrate a margin of operation between 5.5 and 9 dB beyond the standard for all MCS operating modes. Specifically, for MCS12 and MCS0, the sensitivities are −59 and −83.5 dBm, respectively. Within just MCS12, the peak 16-QAM operating mode, Fig. 13(d) shows the sensitivity for each channel, with the worst-case margin being approximately 5.9 dB on channel 2. The figure also shows the nominal "best-case" EVM for MCS12 in each channel when operating under high-SNR conditions. The results range from −22 dB in channel 1, to −20 dB in channel 4.

C. Over-the-Air Link Testing

Finally, link-testing was carried out in the open-air using the antenna-integrated package and the transceiver IC. Testing was carried out in an indoor office-space environment with cubicles and other standard obstructions present. Transmit data was generated using an Agilent AWG, and baseband capture of the received signals was performed by an Agilent oscilloscope. A block diagram of the test-setup is shown in Fig. 14(a).

Results are shown in Fig. 14(b) for LOS links, where a distance of 5.9 m was achieved at MCS12 (16-QAM, 4.62 Gbps) and 20 m at MCS9 (QPSK, 2.5 Gbps). Results from other published works are also shown in the figure.

VI. Performance Summary and Competitive Comparison

Table I shows a comparison between this work and other published 60 GHz systems. Emphasis was placed on reported link results through free-space and results that included package- or substrate-integrated antennas. Both phased-array and single-element devices are represented. The comparison indicates that this work is able to surpass, to the best of our knowledge, all other published single-element designs, and is competitive with some phased-array solutions. Further, if the relative power and area of the different solutions are considered, it is clear that the achieved range and data-rate of this work is an improvement of the state of the art. The realized link distance of [5] requires 6× the radio area, and twice the DC power consumption. Similarly, [1] reaches excellent link distances for a very modest power-consumption increase (relative to this work), but the required radio area is greater than 10× this solution. These results indicate that the cost, in terms of power and area, of achieving high performance 802.11ad/WiGig links through the use phase-array architectures will be high, regardless of the realized system performance improvements.

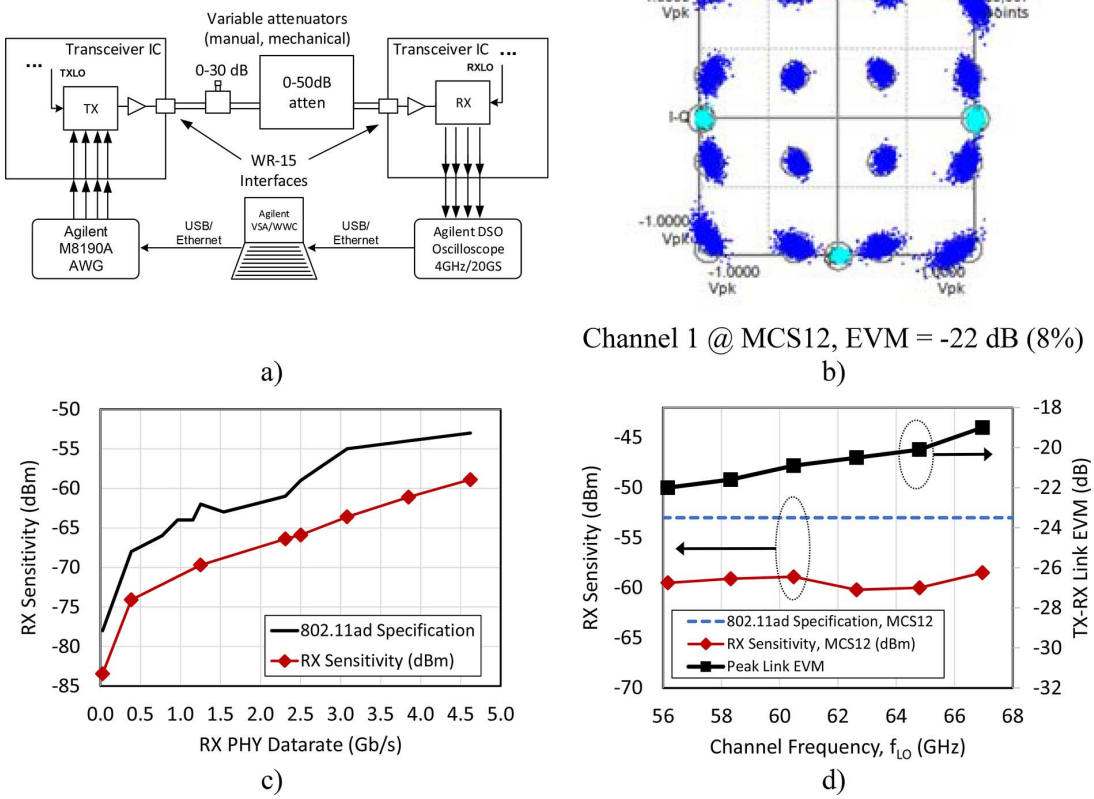

Fig. 13. Measured transmit-receive link setup (a) along with a sample TX-RX link EVM result (channel 1, high SNR) in (b). (c) Receiver sensitivity is shown against the standard specification. (d) TX-RX link EVM results for all channels (under high SNR conditions) along with receiver sensitivity performance for all channels at MCS12 (shown against the −53 dBm specification requirement).

VII. Conclusion

A fully integrated 60 GHz transceiver has been presented in a 130 nm SiGe BiCMOS technology. Functioning across the whole 60 GHz frequency band (57–66 GHz), the system implements a transmitter with an $OP_{1dB}>+13.5$ dBm, a receiver with a noise-figure below 5.5 dB, and a PLL with an integrated RMS error below 7°. Additionally, system-level testing shows transmit EVM results better than −24 dB (corresponding to a ∼3 dB margin), and a receive sensitivity at least 5.5 dB better than the standard requirement for all channels and modulation schemes up to 16-QAM (MCS12). Finally, free-space TX-RX link testing using the package-integrated antenna shows excellent range results with 5.9 m at 4.62 Gbps (MCS12) and over 20 m at 2.5 Gbps. These results represent, to the best of our knowledge, the best published link results for a single-element 802.11ad/WiGig compliant transceiver.

Appendix

A simple system model, based on a link budget analysis, can be used to estimate link distances, especially in the case of line-of-sight configurations. For a simple line-of-sight situation where a basic propagation loss index of 2 is assumed, only the receiver sensitivity must be known in order to examine the potential link distance for a variety of radio configurations. In this case, the receiver sensitivity is defined at a 1% packet-error rate (PER). This number can be determined in a number of ways, either from the minimum specification defined by the standard,

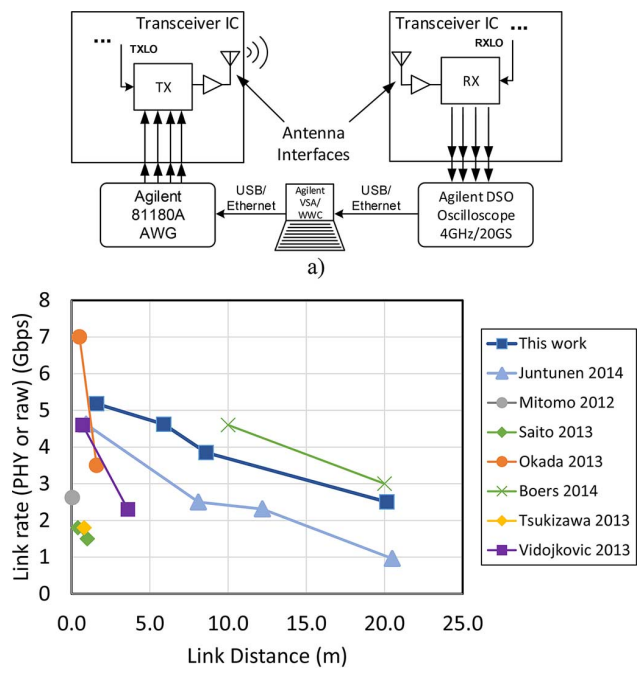

Fig. 14. Link distance testing setup (a) and results from the testing (b), including results from the published literature. Only results that utilize package- or substrate-integrated antennas have been included (excluding external horn antennas, etc.). Raw data-rates vs. PHY data-rates have been used interchangeably here as the specific reporting is not always consistent. One result, [1], is not shown in the plot for scaling purposes, even though the result of 50 m@3.8 Gbps is excellent.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Ref	**This work**	[3]	[5]	[8]	[10]	[27], [28]	[9]	[1]
Process	**130nm SiGe**	130nm SiGe	40nm CMOS	90nm CMOS	40nm CMOS	120nm SiGe	65nm CMOS	65nm CMOS
Channels	**>4**	3	4	4	3	4	4	2
Die Area (mm^2)	**4.97**	4.41	26.3	13.5	12.5	81.5	17.64	72.7
Package Area (mm^2)	**49**	49	–	100	–	1568	234.72	–
Architecture	**1TX, 1RX**	1TX, 1RX	16TX, 16+1RX	1TX, 1RX	4TX, 4RX	16TX, 16RX	1TX, 1RX	32TX, 32RX
TX P_{DC} (mW)	**720**	340	1190	347	584	3800	319	1820
RX P_{DC} (mW)	**340**	285	960	274	400	1800	223	1250
TX OP1dB (dBm)	**13.4 – 16.2**	8	5.2 (single PA)	3.7	10.8	9–13.5	-2	9 (single PA)
Antenna Gain (dBi)	**8**	8	5	6.5	7.5	8	6	–
TX EVM (dB)	**-25**	-22	-25	-22	–	–	–	–
RX Gain (dB)	**70 – 72**	70	–	60	45	70	23	–
RX NF (dB)	**3 – 5**	5	<10	7.1	7.9-8.7 (SSB)	7.4	6	<10
TX-RX EVM (dB)	**-20.5**	–	-19.5	–	-15	-19	-21	-19.2
PN @ 1 MHz (dBc/Hz)	**-89 to -87**	-87	-97.2	-93	-20.3 (int.)	-90.6	-95	-96
Link Dist.(m) / PHY Rate (Gbps)	**20 / 2.5**	8.1 / 2.5	20 / 3.0	1.0 / 2.3	3.6 / 2.3	9 / 5.3*	1.6 /3.5^	184 / 1.9
	5.9 / 4.6	0.93 / 4.6	10 / 4.6	0.4 / 2.5	0.7 / 4.6	9 / 4.5*	0.5 / 7^	50 / 3.8
P_{DC} / Distance (mW/m)	**53.0**	77.2	107.5	621.0	273.3	622.2	338.8	16.7
P_{DC} × Si Area / Distance ($mW \times mm^2$/m)	**263.4**	340.3	2827.3	8383.5	3416.7	50711.1	5975.6	1213.0

*At Link EVM < -18 dB
^Raw data rates

through system simulations of the receiver and the baseband, or, as in this example, through hardware measurements. The sensitivity figure effectively encompasses a number of important parameters including: system noise-figure, implementation losses, thermal noise, and signal bandwidth. It typically ignores nonlinearities on both the transmit and receive sides.

For the case of MCS (modulation and coding scheme) 9, which results in an effective PHY data rate of 2.5 Gb/s, the receiver sensitivity (S_{RX}) for this work, as shown in Section V.B. and in Fig. 13(c), is approximately -66 dBm. With this number, a basic link margin analysis can be carried out:

$$P_T + G_{\mathrm{TX}} + G_{\mathrm{RX}} = S_{\mathrm{RX}} + \mathrm{FSPL} \tag{1}$$

where $P_T, G_{\mathrm{TX}}, G_{\mathrm{RX}}$, and FSPL are the transmit power, transmit antenna gain, receive antenna gain, and free-space path loss, respectively. The first three parameters will all be known based on a specific radio configuration, and the sensitivity is as given above. The FSPL, for ideal conditions assuming no additional atmospheric absorption (i.e., from oxygen or water), is given by:

$$\mathrm{FSPL} = 10 \cdot \log_{10} \left(\frac{4\pi}{c} df \right)^n \tag{2}$$

where c is the speed of light, f is the center frequency of the channel, d is the distance, and n is the propagation loss index, which we take to be 2. The assumption to ignore atmospheric

absorption, which could be as high as 20 dB/km in the 60 GHz band, only applies to links on the order of 50 m or less, where the total effective absorption would amount to 1 dB or less. Solving for situations with longer links, where this assumption cannot be made, requires the use of a full path-loss equation that includes losses from atmospheric effects, and which can no longer be solved as a closed-form expression. However, simple numerical techniques can easily solve such a problem.

For the case where the expected link distance is below 50 m, and using parameters from this work, with $G_{\mathrm{TX}} = G_{\mathrm{RX}} =$ 8 dBi and a transmit power, P_T, of $+13$ dBm, the only unknown for formula (1), is the distance, d. The expression can be rearranged and solved for d:

$$20\cdot\log_{10}(d) = P_T + G_{\mathrm{TX}} + G_{\mathrm{RX}} - S_{\mathrm{RX}} - 20\cdot\log_{10}(f) - 20\cdot\log_{10}\left(\frac{4\pi}{c}\right) \quad (3)$$

$$d = 22.35\ \mathrm{m}. \quad (4)$$

This result compares well with the measured link distance of approximately 20 m.

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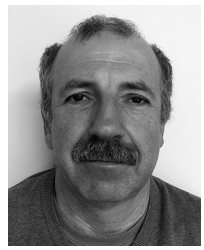

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Hatem Tawfik, photograph and biography not available at the time of publication.

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