entire WLAN band. An axial ratio bandwidth of 2.8% with the same center frequency of 5.77 GHz for CP modes was achieved. A simple dc bias network controlling the polarization states is applied to the antenna prototypes. The reconfigurable U-slot antenna has the further advantages of being compact and easy to manufacture, which makes it highly suited to the advanced wireless communication system.

ACKNOWLEDGMENT

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High-Efficiency On-Chip Dielectric Resonator Antenna for mm-Wave Transceivers

Mohammad-Reza Nezhad-Ahmadi, Mohammad Fakharzadeh, Behzad Biglarbegian, and Safieddin Safavi-Naeini

***Abstract*—A high radiation efficiency on-chip antenna is presented in a low-resistivity silicon technology. The proposed antenna configuration consists of a high-permittivity rectangular dielectric resonator excited by an H-slot antenna implemented in a silicon integrated circuit process. Using the Wheeler method an efficiency of 48% has been measured for the integrated antenna at 35 GHz. The maximum size of this low profile antenna ($h = 0.5$ mm) is close to $\lambda_0/5$ (considering the dielectric resonator), and its radiation gain is around 1 dBi at 35 GHz. Moreover, the bandwidth of this antenna is 4.15 GHz (12%). Simulations and measurements show that by removing the passivation layer on top of the H-slot aperture the radiation efficiency increases by 10%.**

***Index Terms*—Antenna efficiency, millimeter wave antennas, on-chip antennas, silicon, SiGe, slot antenna.**

I. INTRODUCTION

On-chip antennas are essential for implementing fully integrated radio systems. An on-chip antenna significantly simplifies the matching network and improves the system performance through reducing the front-end loss and noise figure. Many of the on-chip antennas take advantage of low-cost semiconductor processing technologies, such as silicon-germanium (SiGe) and complementary metal oxide semiconductor (CMOS) due to their maturity and high integration capabilities [1], [2]. To radiate the maximum amount of the input power or extend the battery life the efficiency of the antenna must be as high as possible. On the other hand, the on-chip antenna dimension is the dominant factor in determining the chip area; hence, its size must be as small as possible to lower the fabrication cost. Antenna miniaturization can be performed by using compact configurations such as H-slot or employing high permittivity material. Miniaturizing the antenna while maintaining a high radiation efficiency is a challenge [3].

This communication reports the design procedure and the measured results of a high-efficiency electrically small integrated antenna. In the proposed configuration an H-slot aperture is used to excite a high-permittivity dielectric resonator (DR) placed on top of the radio chip. The effect of removing the passivation layer (PL) on top of the slot-antenna on the efficiency of the antenna is experimentally studied. The simulated efficiency of the proposed on-chip antenna is 59%. Measured results based on the Wheeler method verify that the radiation efficiency of this system is more than 48%. This is, to the authors' knowledge, the *highest measured* efficiency for an on-chip antenna in low resistivity silicon λ.

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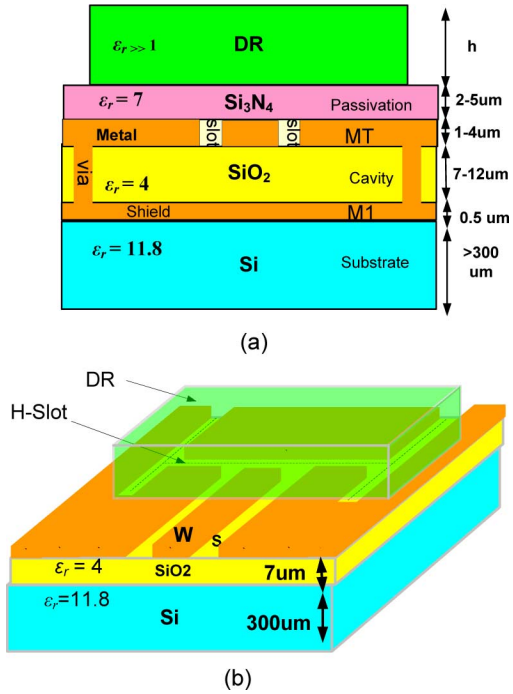

Fig. 1. On-chip cavity backed slot antenna with dielectric resonator on top. (a) Cross section. (b) 3D structure (without the passivation layer).

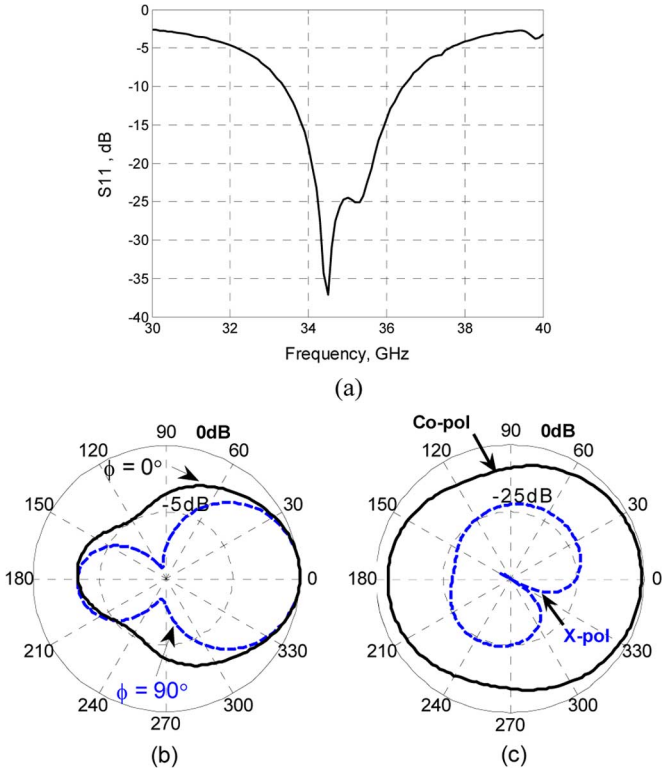

Fig. 2. (a) Simulated reflection coefficient of the on-chip antenna with the DR. (b) 2D normalized radiation patterns. (c) Co-pol and Cross-pol patterns.

II. On-Chip Antenna Configuration

Any improvement in the antenna efficiency results in a larger transmission range for a fixed input power, or less power consumption for a fixed transmission range. This section proposes a configuration to increase the efficiency of the on-chip antenna and reduce the crosstalk to other circuits on the same substrate.

A. Proposed On-Chip Antenna Structure

Fig. 1 illustrates the proposed configuration for the integrated on-chip antenna, which consists of: silicon substrate, cavity and shield layer, H-slot aperture, the passivation layer, and DR. The thickness of silicon substrate is about 300 μm, and its resistivity is 13.5 Ω -cm. The slot aperture is implemented on the top metal layer (MT) of the silicon technology. The lowest metal layer (M1) is connected to the top ground plane through via holes. By shielding the antenna from the lossy silicon substrate, the antenna substrate is limited to silicon dioxide (SiO_2) and the intermediate dielectric layers between metal layers. Also, a cavity is formed under the slot antenna. In Section III, it is shown that the PL can be removed for more efficient power coupling to the dielectric resonator. Finally, a dielectric layer with a large permittivity is placed on top of the chip to increase the radiation efficiency and improve the antenna matching.

B. H-Slot Antenna and Dielectric Resonator

H-slot is an aperture-type electrically small antenna. A slot aperture can be end-loaded to reduce its overall length at a given resonance frequency [4]. For example, in this work the maximum size of the slot antenna is 1.15 mm and the measured resonance frequency is 35 GHz. Thus, the overall length of the antenna is almost $\lambda_0/8$, or 4 times smaller than a half-wavelength dipole operating at the same frequency. The radiation efficiency of such an electrically small antenna is small. To improve the radiation efficiency of the integrated antenna, a layer of high dielectric constant material is added on top of the slot aperture to create a rectangular DR antenna [5]. The slot behaves like a magnetic current, which excites the first order mode of the dielectric resonator in the proposed structure. Thus, the integrated antenna can radiate a larger portion of the input power.

C. Simulation Results

The H-slot was designed and optimized to have a resonance frequency close to that of the rectangular DR. The length, width, height, and dielectric constant of the DR are respectively 1.6 mm, 1.1 mm, 0.5 mm, and 38. Fig. 2(a) shows the simulated reflection coefficient of the on-chip antenna with DR for the $\mathrm{TE}_{11\delta}$ mode. The resonant frequency is 34.5 GHz and the 10 dB bandwidth of the on-chip antenna is more than 3 GHz. The 2D radiation patterns in $\varphi = 0^\circ$ and $\varphi = 90^\circ$ planes of the antenna are shown in Fig. 2(b). The antenna pattern covers the upper half plane and the maximum gain of the antenna structure is 1.06 dBi. Furthermore, the half-power beamwidth of the on-chip antenna exceeds 130° in $\varphi = 90^\circ$ plane. Fig. 2(c) shows that the cross-polarization pattern is at least 20 dB below the co-polarization pattern at the resonant frequency.

III. Measurement Results

Fig. 3(a) shows the die micrograph of the fabricated H-slot antenna and its dimensions. The H-slot antenna was implemented using the IBM SiGe5AM process. Two vertical slots in Fig. 3(a), which constitute the radiating sections of the antenna, have 500 μm length and 100 μm width. The horizontal sections on the top and bottom, which load the radiating slots, are 1 mm long and their width is 50 μm. While the allocated silicon area for the implementation of antenna is 2 mm × 1.5 mm, the largest antenna dimension is only 1.15 mm. The feed network, shown in Fig. 3(a), is a CPW line with 850 μm length, which is probed with Micro-tech CPW probes for test purpose.

In Fig. 3(b) a rectangular DR is placed over the slot to improve the radiation efficiency. The DR used in this work had a dielectric constant of 38 ± 1 and a size of $a = 1.6$ mm, $b = 1.15$ mm, and $h = 0.5$

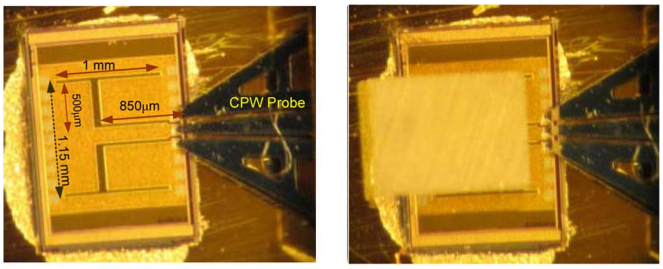

Fig. 3. (a) The dimensions of the H-slot aperture. (b) Die micrograph of the H-shape slot with DR and CPW probe.

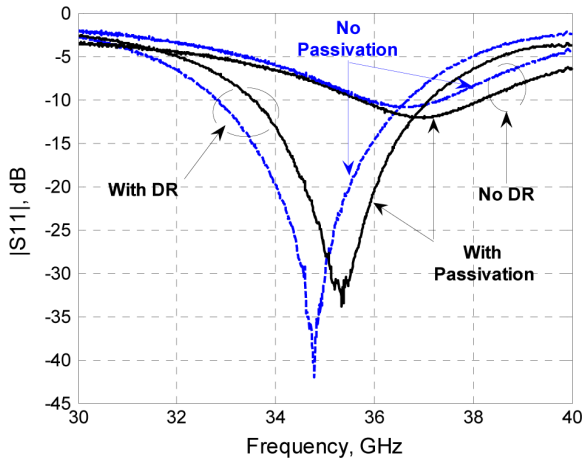

Fig. 4. Measured reflection coefficient of the on-chip antenna with and without the passivation layer (with and without the DR).

mm. Nine samples of on-chip antenna were fabricated and measured: four samples with the PL and five without this layer. The DR was not glued to the H-slot antenna. In the following, the measured results of the different parameters of the fabricated antennas are presented.

A. Resonance Frequency

The first test comprised of measuring the reflection coefficient of the antenna with/without the DR and the PL.

Fig. 4 shows the PL effect on the resonance frequency of the on-chip antenna. Removing the PL decreases the resonance frequency by less than 0.5 GHz. The resonance frequency of the sample without the PL shown in this figure is 34.8 GHz with the DR and 36.5 GHz without the DR.

B. Radiation Pattern Measurement

The radiation pattern measurement setup is shown in Fig. 5. To measure the radiation pattern, a standard gain horn antenna (SGH) was rotated above the on-chip antenna and the received power level by the horn antenna was recorded for each angle. The recorded data was calibrated using the SGH pattern, to find the radiation pattern of the desired structure. The rods and everything around the measurement setup were covered with wave absorbers to avoid any reflected signal. With this method, only the upper hemisphere radiation pattern of the antenna can be measured. Using the described test set-up the radiation pattern at $\varphi = 90^\circ$ plane (y-z plane) was measured. The simulation and measurement result are shown in Fig. 6. The measured half-power beamwidth of the on-chip antenna is close to 110° compared to the simulated value

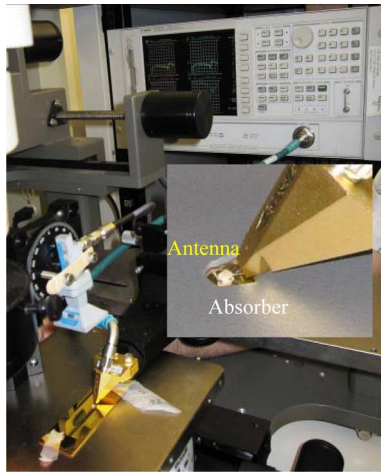

Fig. 5. Radiation pattern measurement set-up for the on-chip antenna. The inset shows the CPW probe coupled to the antenna under test surrounded by wave absorber.

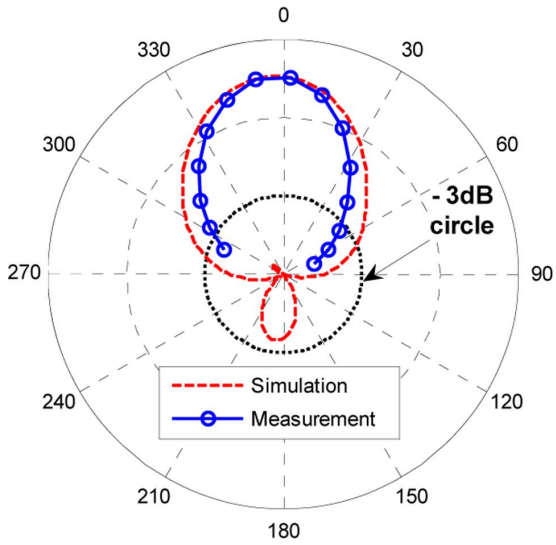

Fig. 6. Normalized measured and simulated radiation patterns of the antenna at 35 GHz. The -3 dB circle is used to find the beamwidth of antenna.

of 130°. Part of this difference is due to the larger ground size of the fabricated samples compared to the simulated model. The rest can be explained by the limited number of the measured points (15 points), and the measurement error.

C. Gain Measurement

The set-up shown in Fig. 5 was used to measure the radiation gain of the antenna. Port 1 of the network analyzer was connected to the SGH, and Port 2 to the CPW probe which fed the on-chip antenna. All scattering parameters were measured with and without the DR. The return loss of the SGH was more than 10 dB over 30–40 GHz range. The measured S_{12} increased significantly by overlaying the DR on the H-slot antenna. Fig. 7 shows the improvement in the received power within the 10 dB bandwidth of the on-chip antenna (33–37 GHz). The improvement varied from 6 dB to 17 dB (after removing the effect of the measurement background noise). The average improvement over the whole 10 dB bandwidth was 12.7 dB

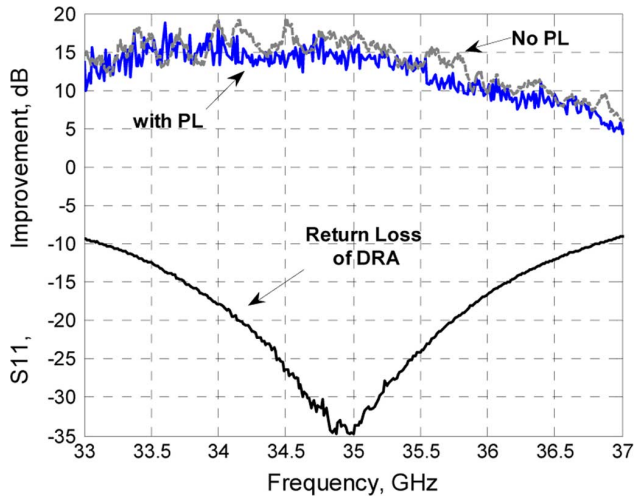

Fig. 7. Measured improvement in the received power by the horn antenna after laying the DR on the H-slot, over the 10 dB bandwidth of the antenna.

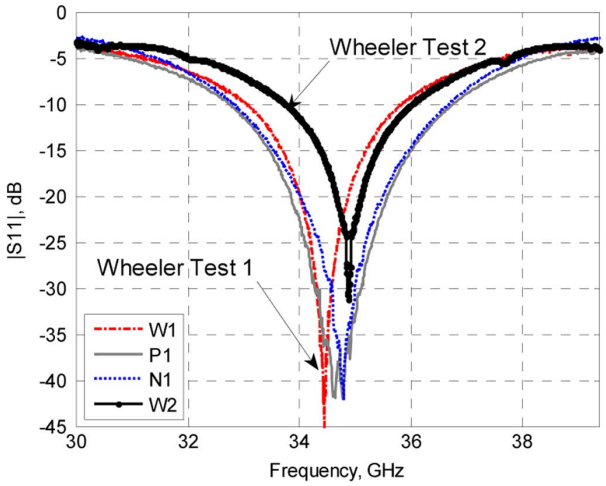

Fig. 8. The Wheeler test results. W1: with the PL and with cap, P1: with the PL-no cap, N1: no passivation-no cap, W2: no passivation with cap.

with the PL and 13.7 dB without the PL. The S-parameter measurements were used to estimate the gain of the on-chip antenna through the following relation [6]:

$$\frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_{\mathrm{Horn}} \cdot G_{\mathrm{On-Chip}} \left(\frac{\lambda}{4\pi R}\right)^2 \quad (1)$$

where R is the distance between the horn and on-chip antennas ($R = 19.5$ cm in this test). In (1) it has been assumed that all sources of insertion loss from port 1 to port 2 of VNA have been compensated, otherwise the uncompensated insertion loss in the test set-up must be added to the right-side of (1).

The unbiased product of horn and on-chip antenna gains derived from (1) is 15 dBi at 35 GHz. The maximum gain of horn antenna at 35 GHz is 15.5 dBi. There is 1 dB insertion loss for the coaxial to waveguide adapter, which connects the horn antenna to the RF cable of the network analyzer. Considering the adapter loss and the polarization mismatch the measured gain of the on-chip antenna at 35 GHz is above 0.5 dBi, which is in good agreement with the simulated gain of 1.06 dBi in Section II.C.

D. Efficiency Measurement

In this part, the Wheeler method is used to measure the efficiency of the on-chip antenna [7]. The Wheeler cap used in this work comprised of a cylindrical cavity, with 10 mm diameter and 8 mm depth, grooved in an Aluminum cube. A small opening was made for the CPW probe. To apply the Wheeler method, the reflection coefficient (S_{11}) of the on-chip antenna system (with the DR) was measured twice: with and without the Wheeler cap.

Then 10 dB fractional bandwidth of the antenna (BW) was calculated in each case, and then the Q factor was found from the following relation [8]:

$$Q = \frac{v-1}{\sqrt{v}\mathrm{BW}} \quad (2)$$

where v is the voltage standing wave ratio. Let Q_W and Q_0 denote the Q factors of the DR antenna with and without the Wheeler cap.

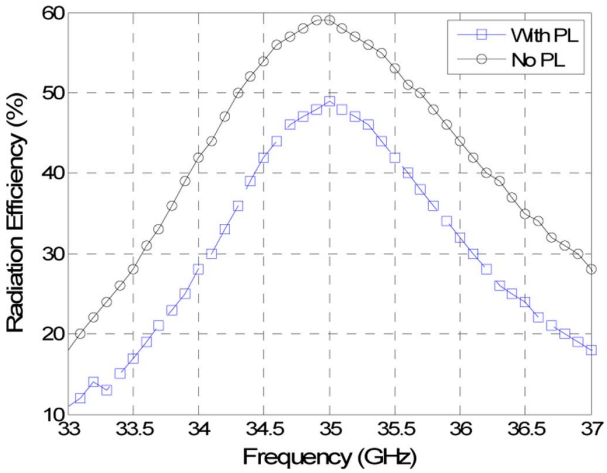

Fig. 9. Simulated radiation efficiency of the entire structure (DR antenna plus chip) which shows a maximum at the resonance frequency.

Then the efficiency at the resonance frequency is calculated from [5]

$$\eta = 1 - \frac{Q_0}{Q_W}. \quad (3)$$

Fig. 8 shows the results of the efficiency measurement test for the antenna with and without the PL. For the former case the values of Q_0 and Q_W are calculated as 5.4 and 8.7. Thus, the efficiency for the DR antenna with the PL is more than 38%. The values of Q_0 and Q_W for the antenna without the PL are calculated as 5.9 and 11.5. Thus, the radiation efficiency is more than 48%. These results show that removing the PL increases the on-chip antenna efficiency by 10%.

To find the efficiency of the proposed on-chip antenna at other frequencies, an EM simulator (HFSS) is used to integrate the received power on a closed surface. Measured results were used to modify the antenna model. Fig. 9 shows the simulated efficiency with and without the PL for a frequency range of 33 to 37 GHz. The maximum efficiency with the PL is 49% at 35 GHz and 59% without the PL at 34.9 GHz. In full agreement with measured results the efficiency increases by 10% when the PL is removed. The 11% difference between the maximum

simulated and measured efficiency is caused by the small opening in the Wheeler cap, Wheeler cap loss, possible shift of the DR after placing the cap atop the antenna, and the measurement/calibration errors.

IV. Conclusion

This communication introduced a high-efficiency on-chip antenna in SiGe MiMIC technology. The antenna consisted of an on-chip H-slot antenna and a rectangular dielectric resonator. A shielding mechanism was implemented to isolate the radiating section from the lossy silicon substrate. Using the Wheeler method a radiation efficiency of 48% was measured. This electrically small antenna has a relatively large bandwidth of 12% operating from 33 to 37 GHz. It was shown that adding the high-permittivity rectangular DR, improves the efficiency and matching of the antenna structure by 17 dB. Moreover, it was shown that removing the passivation layer on top of the slot improves the coupling between DR and H-slot antenna, which increases the radiation efficiency by 10%. This result was confirmed by both measurements and simulations.

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Investigation Into the Effects of the Reflection Phase Characteristics of Highly-Reflective Superstrates on Resonant Cavity Antennas

Alireza Foroozesh and Lotfollah Shafai

***Abstract*—First we describe two frequency selective surfaces (FSSs), one capacitive and the other inductive, that are designed to exhibit identical high-reflection magnitude at an arbitrary frequency. These two FSSs are then employed as the superstrate of two RCAs having identical microstrip patch source. In order to determine the resonant conditions and obtain approximate values for the antenna directivity, RCAs are initially analyzed using the well known simple ray-tracing method. Next, a full-wave analyzer (ANSOFT Designer v4.0), based on the method of moments (MoM), is utilized to thoroughly analyze the RCAs. Experimental results are provided to support the full-wave simulations, as well. In contrast to the prediction of the ray-tracing modeling, which is merely based on the reflection magnitude of the FSSs, it is pointed out that their phase properties have noticeable effects on the RCA gain. Second, two other RCAs are designed based on high permittivity and high permeability superstrates with identical contrast. There, too, it is shown that the reflection phases of the RCA superstrates determine the air-gap heights which in turn affect the RCA gains.**

***Index Terms*—Antenna gain, antenna input impedance, antenna radiation patterns, frequency selective surface (FSS).**

I. Introduction

A highly-reflective surface can be used as the antenna superstrate to substantially increase its directivity [1]. The phenomenon resulting in this significant gain enhancement is based on multiple reflections between the highly-reflective superstrate and the antenna ground plane similar to the Fabry-Perot resonator. Using a ray-tracing method, a simple formula has been derived in [1], which shows the relationship between the reflection magnitude of the superstrate and the relative increase in the antenna directivity by adding that superstrate. This simple relationship has been proven to be relatively accurate when highly-reflective capacitive FSSs, such as periodic patches or strips, have been employed as the RCA superstrates [2], [3]. However, the accuracy of this relationship has neither been studied nor verified in the literature, when inductive FSSs are used as the RCA superstrate.

As it is known, the resonance length of the RCA is determined by the reflection phase of the FSS and the ground plane. It has been shown in [4] that for the RCAs whose superstrates are identical high-permittivity dielectrics but their ground planes are PEC and PMC surfaces, the RCA having PEC ground plane produces higher directivity and resonance length. Similar phenomena have been observed in [5], when metamaterial ground planes are utilized in designing RCAs. In [5], it has been shown that the antenna with shorter resonance length exhibits lower directivity. Therefore, the purpose of this communication is to investigate the effects of the reflection phase of the FSS superstrates, as opposed to the ground planes carried out in [4] and [5], on the RCAs directivity. This effect is also studied for the RCAs having high permittivity or permeability superstrate layers.

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