Characterization of Flip-chip Interconnect for mm-wave System in Package Applications

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***Abstract*—This paper describes a systematic approach to characterize flip-chip solder bump interconnects to accurately design mm-wave on-chip devices and matching circuits for on-package components. Variety of on-chip test structures are fabricated and measured from DC to 67 GHz by GSG probes landed on bare and bumped pads. Combination of two double-delay based de-embeding methods are used to calculate the transmission lines (TLs) and interconnect characteristics. Furthermore, scattering parameter of bare pads and bump pads are accurately extracted from measurement results without lumped element assumption.**

***Index Terms*—Flip-chip interconnect, de-embeding method, mm-wave System in package, pad parasitics**

I. Introduction

By emerging new application for mm-wave transceivers, system-in-package (SiP) is the only reliable packaging solution in which the antenna is implemented as a part of package. In mm-wave SiPs, co-design of antenna and front end circuits are essential due to the considerable parasitics caused by interconnects such as solder bumps and vias. Since the antenna input impedance seen from the chip is affected by the interconnect parasitics, as shown in Fig. 1, an accurate modeling of the package interconnect is a crucial part of mm-wave SiP design process [1].

In literature, numerous efforts have been dedicated to propose a robust methods for de-embeding the parasitic effects of interconnects. In this work, two methods are employed together to improve the accuracy of de-embeding. The de-embeding method is briefly explained and the extracted results for TL characteristics and pad and bump parasitics are presented.

II. De-embeding Method

A de-embeding technique is proposed in [2] to extract the characteristic impedance and propagation constant of an on-chip TL by measuring two identical lines with different lengths (l_s, l_l) assuming that the interconnect parasitics is a shut element. Measured scattering parameters for long and short TLs, $S^{m,l}$ and $S^{m,s}$, can be converted to $ABCD$ form at $50\,\Omega$-system denoted by $A_{m,l} = toA\{S^{m,l}\}$ and $A_{m,s} = toA\{S^{m,s}\}$. Then, an auxiliary matrix A_T is defined as

$$A_T = A_{m,l} \times A_{m,s}^{-1} = A_p \times A_{\Delta l} \times A_p^{-1} \tag{1}$$

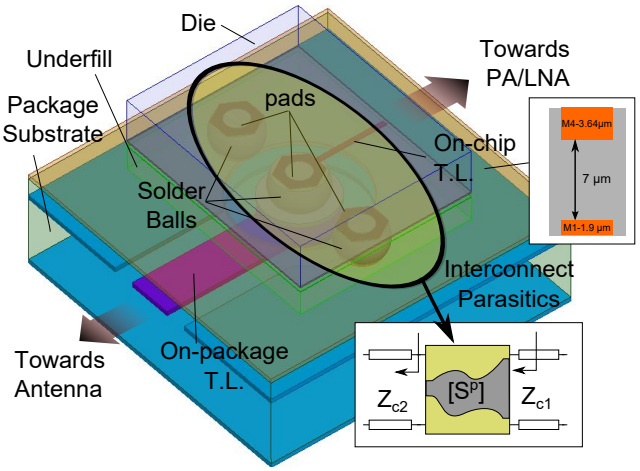

Fig. 1. 3D view of a typical flip-chip packaging technology and interconnect parasitics that causes impedance transformation seen from the die

where $\Delta l = l_l - l_s$, and A_p is $ABCD$ representation of interconnect parasitics. Y-matrix representation of A_T can be defined as $Y_T = toY\{A_T\}$. Moreover, swapped form of Y_T is obtained by changing ports numbering ($1 \leftrightarrow 2$) is represented as Y_T^{swap}. Parallel connection of Y_T and Y_T^{swap} leads to cancellation of shunt parasitic (Y_p), and the remaining is two TLs with Δl length connected in parallel, i.e. $2Y_{\Delta l} = Y_T + Y_T^{swap}$. By transforming $Y_{\Delta l}$ to $ABCD$ form, $A_{\Delta l} = toA\{Y_{\Delta l}\}$, characteristic impedance (Z_c) and propagation constant (γ) of the TL can be calculated as

$$Z_c = \sqrt{\frac{B_{\Delta l}}{C_{\Delta l}}}, \quad \gamma = cos^{-1}(A_{\Delta l}) \tag{2}$$

The described method was based on shunt interconnect parasitics which is fairly valid assumption particularly in low frequencies. However, the characteristics TLs given by Eq. (2) can be used in another method to generally calculate the interconnect parasitics as follows. The scattering parameters measured for each of short and long TLs can be expressed as

$$\begin{aligned} S_{11}^{\text{m},i} &= S_{11}^p + S_{22}^p \frac{(S_{12}^p \Gamma_i)^2}{1 - (S_{22}^p \Gamma_i)^2} \\ S_{12}^{\text{m},i} &= \frac{(S_{12}^p \Gamma_i)^2}{1 - (S_{22}^p \Gamma_i)^2} \end{aligned} \tag{3}$$

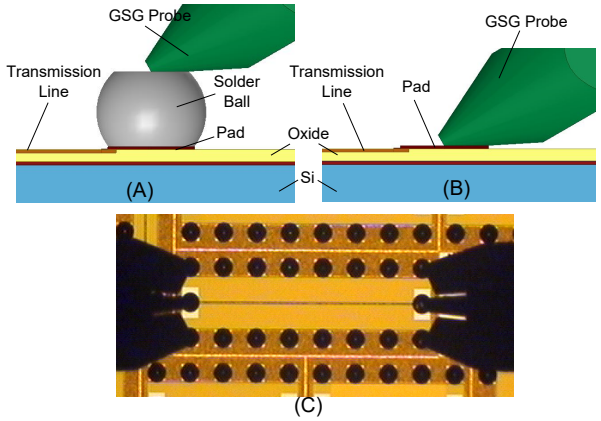

Fig. 2. Side view of landed probe on (a) bare die, (b) bumped die, (c) landed probe on bumped die and die micrograph.

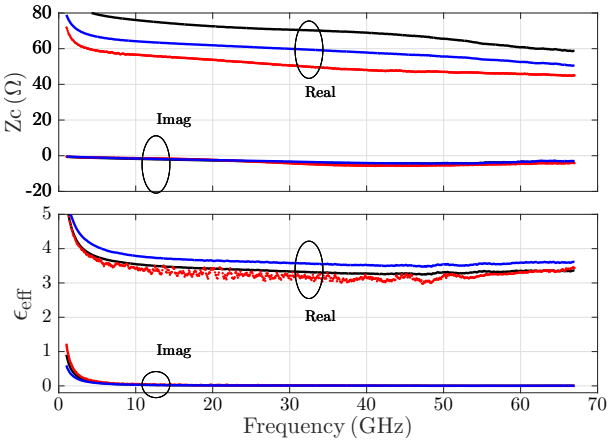

Fig. 3. Extracted TL characteristics from measurement of microstrip lines with $w = 3\ \mu m,\ 6\,\mu m,\ 10\,\mu m$ shown in black, blue and red. respectively

where index $i(= s \text{ or } l)$ represents short and long TLs, respectively, and $\Gamma_i = e^{\gamma l_i}$ is the delay of the TL and Four equations can be solved analytically with respect to $S_{11}^p, S_{12}^p, S_{22}^p, \gamma$ [3]. It must be noted that matched transmission lines assumption is used to derived Eq. (3), therefore, measured scattering parameters must be transformed to the Z_c-base system, where Z_c is obtained from Eq. (2).

III. Measurement Results

A chip with various TLs with different width and lengths is fabricated in CMOS 350nm TSMC technology with 4 metal layers (M1-M4). Three types of microstrip lines are realized with $w = 3\ \mu m,\ 6\mu m,\ 10\mu m$ width on M4 and M1 as ground plane. The designed values of characteristic impedance, calculated by 2D FEM method, are $Z_0 = 60\ \Omega,\ 50\ \Omega, 40\ \Omega$, respectively. The pads are octagons with circumcircle diameter of $100\,\mu m$ and pitch size of $180\,\mu m$. Besides the bare chip, a chip is solder-bumped for measurement purposes. The solder bumps are made in SnAg with around $80\,\mu m$ diameter and $60\,\mu m$ height.

Measurements are performed on probe stations with $200\mu m$-pitch GSG probes connected to N5247A PNA-X vector network analyzer and calibrated by line-reflect-match (LRM) algorithm. The probes are landed on pads of bare dies and on top surface of the solder bumps of the bumped chips as shown in Fig. 2.

A. On-chip Transmission Lines

By applying described method in Section III, TL characteristics are extracted from the measurements data as shown in Fig. 3. The effective dielectric constant of TL is plotted that is defined as $\epsilon_{\text{eff}} = (c\gamma/\omega)^2$, where c is speed of light and ω is angular frequency. The real parts of Z_c are in good agreement with simulated design values particularly at higher frequencies. It should be noted the double delay method seems to fail at lower frequencies due to the small delay difference of the test TLs.

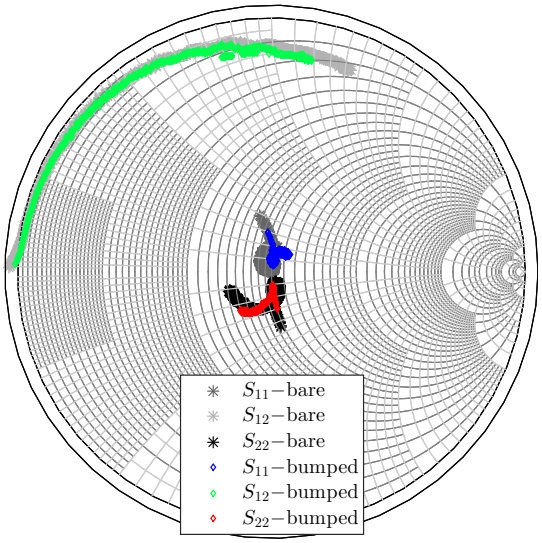

Fig. 4. Extracted scattering parameters of interconnect parasitics for bare pad and bumped pad

B. Unbumped-pad and Bumped-pad Characterization

Eq. (3) is solved for interconnect parasitics for both bare and bumped dies and the results are shown in Fig. 4. It can be observed that the interconnect parasitics show better matching for bare pad compared to pumped. This verifies the fact that the adding bump adds to parasitics of the interconnect.

References

[1] H.-C. Lu, C.-C. Kuo, P.-A. Lin, C.-F. Tai, Y.-L. Chang, Y.-S. Jiang, J.-H. Tsai, Y.-M. Hsin, and H. Wang, "Flip-chip-assembled-band cmos chip modules on ceramic integrated passive device with transition compensation for millimeter-wave system-in-package integration," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 60, no. 3, pp. 766–777, 2012.

[2] A. Mangan, S. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," vol. 53, no. 2, pp. 235–241.

[3] S. Georgakopoulos and S. Ogurtsov, "An s-parameter extraction technique for broad-band characterization of microstrip-to-SIW transitions," in *IEEE Antennas and Propagation Society International Symposium, 2009. APSURSI '09*, pp. 1–4.